

T5S0 Serial Command Screen Application Guide

Contents

1 Overview	3
1.1 User Interface Definition (06 Series COF Screen with 12Pin 0.5mm FPC Interface)...	4
2 Serial Command Set.....	5
2.1 Display Coordinate Basic Definition	5
2.2 Serial Data Frame Format.....	5
2.3 Command Set.....	6
3 Download Mode.....	18
4 Hardware Configuration File Format (*.CFG).....	21
5 T5S0 Chip Package Definition (4×4mm QFN48 Package).....	23
6 OS CPU Function Module Programming Description.....	25
6.1 Initialization Configuration.....	25
6.2 Memory.....	25
6.3 Multiplication/Division Unit (MDU).....	31
6.4 Timer	33
6.5 Watchdog Timer (WDT).....	34
6.6 Pulse Width Modulation Module (PWM).....	35
6.7 I/O Ports	37
6.8 AD Conversion	38
6.9 UART Communication Interface	40
6.10 Interrupt System	40
Revision Record	43

1 Overview

The T5S0-based serial command screen adopts DWIN's low-cost, low-power T5S0 ASIC as the core design. It supports LCD panels with resolutions of 480×320 and below via QSPI or 8080 parallel interface. It is mainly designed for upgrading low-cost digital tube and segment LCD displays.

Features:

- 65K-color display (Colors are configured as 24-bit color in serial commands).
- Basic drawing commands; scalable display for Chinese and ASCII text. Supports JPEG icons, barcodes and QR codes.
- External support for up to 16Mbytes SPI NOR Flash (4Mbytes as standard).
- 32Kbytes SRAM data memory readable and writable via serial port.
- 32Kbytes Flash data memory readable and writable via serial port; data is retained after power-off, with a write endurance of 100,000 cycles.
- Supports serial port configuration of parameters and updating of font libraries, image libraries and codes.
- Built-in display memory; display refresh is controlled via serial port, facilitating high-quality UI design.
- Serial communication speed up to 7.3728Mbps, supports user-defined baud rates and CRC data check.

1.1 User Interface Definition (06 Series COF Screen with 12Pin 0.5mm FPC Interface)

PIN#	Definition	I/O	Description	Remarks
1	GND	P	GND, internally paralleled.	
2	GND	P		
3	+3.3	P	3.3V power supply, internally paralleled.	DC 3.2-3.4 V, 200 mA.
4	+3.3	P		
5	RXD	I	UART input.	3.3V CMOS/TTL level serial port. Internal 10K pull-up, followed by a 100R series resistor to the interface.
6	TXD	O	UART Output.	
7	TDO	O	Floating, do not use.	Internal 10K pull-up, followed by a 100R series resistor to the interface.
8	TDI	I		Internal 10K pull-up, followed by a 100R series resistor to the interface.
9	TCK	I		Internal 10K pull-up, followed by a 100R series resistor to the interface.
10	TMS	I		Internal 10K pull-up, followed by a 100R series resistor to the interface.
11	JIOS	I		Internal 10K pull-up, followed by a 100R series resistor to the interface.
12	CFG	I	Operating mode selection.	Internal 10K pull-down, followed by a 100R series resistor to the interface. Upon power-up, T5S0 performs detection to determine the operating mode: Low level or floating: Operates with user-configured serial port settings. High level: Serial port baud rate=921600 bps, 8N1, no CRC check.

2 Serial Command Set

2.1 Display Coordinate Basic Definition



2.2 Serial Data Frame Format

The serial port is fixed to 8N1 mode, and the baud rate is user-configurable.

The serial data frame consists of four parts: frame header, command, data, CRC check, and frame terminator, as described in the table below:

Frame Header	Command	Data	CRC Check (Optional)	Frame Terminator
Fixed at 0xAA	1 byte, refer to the command set description	Max. 248 bytes	CRC check of command and data	Fixed at 0xCC 33 C3 3C

2.3 Command Set

(1) Configuration and Interface Command

Function	Command	Data	Description
Handshake	0x00	Transmit: None Response: 0x4F 0x4B Version Config	Version: Software Version number. Config: Value at address 0x0012 of system configuration file (.CFG). Example: Tx: AA 00 CC 33 C3 3C Rx: AA 00 4F 4B 10 00 CC 33 C3 3C
CRC Report	0xFF	0x01	When serial CRC check is enabled, this command will be automatically responded if CRC verification fails.
Backlight Brightness Adjustment	0x30	DIM_Set	DIM_Set: Backlight brightness value. 0x00 (off)~ 0xFF (full brightness). Example: Tx: AA 30 80 CC 33 C3 3C Brightness set to 50%.
Write Data Memory	0x31	Transmit: 0x5A, Address, Datas Response: 0x5A 0x4F 0x4B Response after successful write.	Address: Address for writing to the 32KB SRAM data memory, range 0x0000~0x7FFF. Datas: Data bytes to be written. Example: Tx: AA 31 5A 00 00 31 32 33 34 CC 33 C3 3C Rx: AA 31 5A 4F 4B CC 33 C3 3C
Read Data Memory	0x32	Transit: 0x5A, Address, Length Response: 0x5A, Address, Length, Datas	Address: Address for reading from the 32KB SRAM data memory, range 0x0000~0x7FFF. Length: Number of data bytes to read, range 0x01 ~ 0xF0. Datas: Read data bytes. Example: Tx: AA 32 5A 00 00 04 CC 33 C3 3C

Function	Command	Data	Description
			Rx: AA 32 5A 00 00 04 31 32 33 34 CC 33 C3 3C
Refresh Display	0x3D	Transit: None Response: 0x4F 0x4B Response is sent after refresh completes.	Refresh the display once (update T5S0 display buffer content to the LCD panel). Example: Tx: AA 3D CC 33 C3 3C Rx: AA 3D 4F 4B CC 33 C3 3C DMT32240F028-06WN: It takes approximately 10 ms to execute this refresh command.
On-chip Flash Data Save / Load	0x3E	Transmit: 0x5A, 0xA5, 0x00, Mode Response: Mode, 0x4F, 0x4B Response after processing completes.	Mode=0x55, Load data from Flash. Read data from the on-chip 32KB Flash into the 32KB SRAM data memory. Data loading takes approximately 32 ms. Example: Tx: AA 3E 5A A5 00 55 CC 33 C3 3C Rx: AA 3E 55 4F 4B CC 33 C3 3C Mode=0xAA, Save data to Flash. Save data from the 32KB SRAM data memory to the on-chip 32KB Flash .If power failure occurs during data saving, the original data will be automatically restored. Maximum data saving time: 3 seconds. Example: Tx: AA 3E 5A A5 00 AA CC 33 C3 3C Rx: AA 3E AA 4F 4B CC 33 C3 3C
Enter Download Mode	0x3F	Transit: 0x5A A5 BODE_SET Response: 0x4F 0x4B	BAUD_SET: Configures the serial baud rate for download, 4 bytes.

Function	Command	Data	Description
		T5S0 switches baud rate and enters download mode.	Minimum baud rate: 9600bps (0x00002580); Maximum baud rate: 7372800bps (0x00708000). Example: Tx: AA 3F 5A A5 00 0E 10 00 CC 33 C3 3C Rx: AA 3F 4F 4B CC 33 C3 3C Enter download mode and set the baud rate to 921600bps.

(2) Drawing Related Commands

Command	Data	Description
0x01	Color	Clear screen. Color: Screen clearing color, configured in 24-bit RGB. Example: AA 01 00 00 FF CC 33 C3 3C DMT32240F028-06WN: It takes 0.25 ms to execute this example command.
0x02	Color, N, (X0, Y0) ... (Xn, Yn)	Draw pixels. Color: Pixel color, configured in 24-bit RGB. N: Pixel size. The actual pixel dimension of each point is $N \times N$, range 0x01 ~ 0x0F. (Xn, Yn): Coordinate sequence of pixels. Example: AA 02 FF 00 00 04 00 08 00 08 00 80 00 80 CC 33 C3 3C DMT32240F028-06WN: Execution time of this example command is negligible.
0x03	Color, N, (X0, Y0), ... (Xn, Yn)	Draw lines between endpoints. Color: Line color, configured in 24-bit RGB. N: Line thickness. The pixel size of line segments is $N \times N$, range 0x01~0x0F. (Xn, Yn): Endpoint coordinates of line segments. Example: AA 03 FF FF FF 04 00 08 00 08 00 80 00 80 CC 33 C3 3C DMT32240F028-06WN: Execution time of this example command is negligible.
0x04	Color,N, (X, Y), R AD	Draw circle. Color: Display color. N: Line thickness. The pixel size of line segments is $N \times N$, range 0x01~0x0F.(X, Y): Center coordinates of the circle. RAD: Circle radius.

Command	Data	Description
		Example: AA 04 FF FF FF 01 00 78 00 78 00 60 CC 33 C3 3C DMT32240F028-06WN: It takes 0.22 ms to execute this example command.
0x05	Mode, Color, N, (Xs, Ys; Xe, Ye) ... (Xs, Ys; Xe, Ye) n	Draw rectangular area. Mode: 0x00=Draw rectangular frame with defined Color; line thickness defined by N. 0x01=Fill rectangular area with defined Color. 0x02=XOR paint rectangular area with defined Color, commonly used for menu selected / unselected highlighting. Color: Color configured in 24-bit RGB. N: Line thickness. The pixel size of line segments is $N \times N$, range 0x01~0x0F; valid only in rectangular frame mode.(Xs, Ys; Xe, Ye): Top-left and bottom-right coordinates of the rectangle. Example: AA 05 02 00 FF 00 02 00 08 00 08 00 80 00 80 CC 33 C3 3C DMT32240F028-06WN: It takes 0.1 ms to execute this example command.
0x06	Mode, N, Color0, Color1, Color2, (Xs, Ys), (Xe, Ye), data	Draw rectangular progress bar. Mode: Display mode Bit7: 0=show outer frame; 1=hide outer frame. Bit6: 0=fill background; 1=no background fill. Bit5~Bit2: Reserved, write 0. Bit1~Bit0: Direction. 00=Left to Right; 01=Right to Left; 10=Bottom to Top; 11=Top to Bottom. N: Outer frame line thickness. The pixel size of line segments is $N \times N$, range 0x01 ~ 0x0F. Color0: Outer frame color.

Command	Data	Description
		Color1: Background color. Color2: Progress bar color. (Xs,Ys), (Xe,Ye): Display area of progress bar (outer frame area). Data: Progress value. 0x00~0x64 corresponds to 0%~100%. Example: AA 06 00 02 FFFFFFFF 000000 00FF00 0008 0008 006F 001C 32 CC33 C33C DMT32240F028-06WN: Execution time of this example command is negligible.
0x07	Color0, Color1, (X, Y), R_MAX, R_MIN, DS, DE, data	Draw annular progress bar. Color0: Background color. Color1: Progress color. (X, Y): Center coordinates of the annulus. R_MAX: Outer ring radius, range 0x0001~0x0400. R_MIN: Inner ring radius, range 0x0001~0x0400. DS: Start angle, unit: 0.5° , range 0x0000~0x02D0, rotating clockwise. DE: End angle, unit: 0.5° , range 0x0000~0x02D0, rotating clockwise. data: Progress value. 0x00~0x64 corresponds to 0% ~ 100%. Example: AA 07 FFFFFFFF 0000FF 0078 0078 0070 0040 01C2 010E 32 CC33 C33C DMT32240F028-06WN: It takes 1.7 ms to execute this example command. If R_MIN=0x0000, DS=0x0000, DE=0x02D0 and data=0x00 are set, a solid circle with radius R_MAX will be displayed.
0x09	Mode, DIS, Color, (Xs, Ys), (Xe, Ye)	Selected area movement. Mode: Movement mode

Command	Data	Description
		Bit7: Movement mode. `0 = Wrap-around shift; 1 = Parallel shift, blank area filled with specified color.` Bit6~Bit2: Write 0. Bit1~Bit0: Movement direction. `00=Left, 01=Right, 10=Up, 11=Down.` DIS: Movement distance, number of pixel dots, range `0x0000~horizontal resolution/2`. 2bytes. Color: Fill color, configured in 24-bit RGB. Valid only when Mode.Bit7 = 1. (Xs, Ys), (Xe, Ye): Coordinates of the selected area. Example: AA 09 00 00 08 FF FF FF 00 10 00 10 00 80 00 80 CC 33 C3 3C DMT32240F028-06WN: It takes 0.1 ms to execute this example command.

(3) Text Related Commands

Command	Data	Description
0x12	Lib_ID, Text_V, Mode, Color0, Color1, (Xs, Ys, Xe, Ye), DX, DY, Strings	String display. Lib_ID: Font library ID, range 0x0 0~0xFF. The font library must be processed with DWIN tool software. Text_V: Text size (dot count in vertical direction), range 0x08~0xFF. Auto-scaling supported. Mode: Display mode Bit7: Fill text box with background color before displaying text. 1=Enable fill; 0=No fill. Bit6: Restore text box with original image background before displaying text. 1=Restore; 0=Do not restore. Bit5: Space display size. 1=Text_V/2; 0=Text_V/4. Bit4: Reserved, write 0. Bit3~Bit0: String encoding mode 0=8-bit encoding, 1=GB2312, 2=GBK, 3=BIG5, 4=SJIS, 5=UNICODE encoding Color0: Character display color, configured in 24-bit RGB. Color1: Text box fill color, configured in 24-bit RGB. (Xs, Ys, Xe, Ye): Text box area. DX: Character spacing between each character. DY: Column spacing between each character column. Strings: String to be displayed. The string is displayed left to right and top to bottom within the text box. Example: AA 12 00 20 80 00 00 00 FF FF FF 0010 0010 00C0 0040 01 00 30 31 32 33 34 35 36 37 38 39 CC 33 C3 3C DMT32240F028-06WN: It takes 0.2 ms to execute this example command. (20uS per character on average).
0x13	Lib_ID, Text_V, Mode, Color0, Color1, Num_I, Num_F, (Xs, Ys, Xe, Ye), Datas	Data variable display. Lib_ID: Font library ID, range 0x00~0xFF. The font library shall be processed by DWIN configuration tool.

Command	Data	Description
		When Lib_ID=0xFF, the built-in 8×12 dot matrix font is used by default, and Text_V is invalid. Text_V: Text size (dot count in vertical direction), range 0x08~0xFF, auto scaling supported. Mode: Display mode Bit7: Fill text box with background color before display: 1=Enable fill; 0=No fill. Bit6: Restore text box with current image background before display: 1=Restore, 0=No restore. Bit5: Leading zero display control: 1=Show leading zeros, 0=Hide leading zeros. Bit4: Format for leading zero: 1=Display as '0', 0=Display as space. Bit3~Bit2: Data variable format 00=Unsigned integer 01=Signed integer 10=32-bit single-precision float 11=64-bit double-precision float Bit1~Bit0: Alignment mode 00=Left align 01=Right align 10=Center align Color0: Character color, configured in 24-bit RGB. Color1: Text box fill color, configured in 24-bit RGB. Num_I: Number of integer digits to display, range 0x01~0x14. Num_F: Number of fractional digits to display, range 0x00~0x14. The sum of Num_I and Num_F cannot exceed 20. Datas: Data variable with a maximum capacity of 8 bytes. (Xs, Ys, Xe, Ye): Text box area. Datas: Data variable, max 8bytes. Characters are displayed in a single line, centered inside the text box. Example: AA 13 FF 0C 81 00 00 00 FF FF FF 04 04 0010 0010 0080 0050 00 FF FF FF CC 33 C3 3C DMT32240F028-06WN: It takes 0.12 ms to execute this example command.

(4) Image and Icon Related Commands

Command	Data	Description
0x21	(X, Y), Color0, Color1, QR_Pixel, DATA	QR code display. (X, Y): Coordinates for QR code display. Color0: QR code foreground color, configured in 24-bit RGB. Typically black (0x000000). Color1: QR code background color, configured in 24-bit RGB. Typically white (0xFFFFFFFF). QR_Pixel: Pixel size for each QR code module, range 0x01~0x07. DATA: Data to be displayed, maximum 154bytes. QR code dimension: $(46 \times \text{QR_Pixel}) \times (46 \times \text{QR_Pixel})$ dots. Example: AA 21 00 08 00 08 000000 FFFFFFFF 03 68 74 74 70 3A 2F 2F 77 77 77 2E 64 77 69 6E 2E 63 6F 6D 2E 63 6E CC 33 C3 3C DMT32240F028-06WN: It takes 2.6 ms to execute this example command.
0x22	ICL_ID, JPEG_ID	Full-screen JPEG image display, processing speed: approx. 20ns per pixel. Single JPEG file cannot exceed 76KB. ICL_ID: ID of the ICL file storing JPEG images, range 0x00~0xFF. JPEG_ID: ID of the target JPEG image to display, range 0x0000~0xFFFF. The image displayed by the latest 0x22 command will be used as the current image background for background restoration operations. Example: AA 22 08 00 00 CC 33 C3 3C DMT32240F028-06WN: It takes 1.5 ms to display one 320×240 resolution image with this command (typically 1.3~2.0 ms, depending on JPEG file size).
0x23	ICL_ID, Mode, Color, (Xs, Ys, Xe, Ye), DX, Icon_IDs	JPEG icon display, processing speed: approx. 20ns per pixel. Single JPEG file cannot exceed 76KB. ICL_ID: ID of the ICL file storing JPEG images, range 0x00~0xFF. Mode: Icon display mode.

Command	Data	Description
		Bit7: Fill the icon box with background color before icon display: 1=Enable fill, 0=No fill. Bit6: Restore the icon box with current image background before icon display: 1=Restore, 0=No restore. Bit5: Icon background display setting: 0=Background filtered out and not displayed, 1=Background displayed. Bit4: Reserved, write 0. Bit3~Bit0: Background filtering strength selection (valid only when Bit5=0). 0x0=Weakest, 0xF=Strongest. Color: Icon box fill color, configured in 24-bit RGB. (Xs, Ys, Xe, Ye): Icon box area. The first icon is displayed at position (Xs, Ys). DX: Icon spacing adjustment, range 0x00~0xFF, 8-bit signed integer. Icon_IDs: IDs of icons to be displayed, range 0x0000~0xFFFF. Example: AA 23 08 48 00 00 00 0010 0010 00E0 0080 00 0001 0002 0003 0004 CC 33 C3 3C DMT32240F028-06WN: It takes 1.5 ms to render one 320×240 resolution icon with background enabled. The display time will be shorter when background filtering is enabled (typically 0.8~1.2 ms).
0x24	(x, y), Mode, Address	Data memory JPEG icon display, processing speed: approx. 13ns per pixel. JPEG file cannot exceed 32KB. (x, y): Display position of the icon on the screen. Mode: Icon display mode. Bit7~Bit6: Reserved, write 0. Bit5: Icon background display setting: 0=Background filtered out and not displayed, 1=Background displayed. Bit4: Reserved, write 0. Bit3~Bit0: Background filtering strength selection (valid only when Bit7=0). 0x0=Weakest, 0xF=Strongest. Address: Start address of JPEG icon data stored in data memory, range 0x0000~0x7FFF.

Command	Data	Description
		Example: AA 24 00 10 00 10 00 00 00 CC 33 C3 3C DMT32240F028-06WN: It takes 1 ms to render one 320×240 resolution icon with background displayed. The display time will be shorter when background filtering is enabled (typically 0.3~0.7 ms).
0x2A	(X, Y), DATA	EAN-13 barcode display. (X, Y): Coordinates for barcode display. DATA: 12 bytes of barcode data, HEX encoded (0x00~0x09). Barcode module width is fixed at 2 pixels. The total barcode area is 222×94 dots. Example: AA 2A 00 08 00 08 09 07 08 07 05 03 09 09 08 03 02 04 CC 33 C3 3C DMT32240F028-06WN: It takes 0.6 ms to execute this example command.
0x2C	ICL_ID, JPEG_ID, (Xs, Ys, Xe, Ye), (x, y)	Copy the specified area from a JPEG image and paste it to the target position on the current display. Single JPEG file cannot exceed 76KB. ICL_ID: ID of the ICL file storing JPEG images, range 0x00~0xFF. JPEG_ID: ID of the target JPEG image, range 0x0000~0xFFFF. (Xs, Ys, Xe, Ye): Area on the JPEG image. (x, y): Target position to paste the copied area. Example: AA 2C 03 00 01 00 08 00 08 00 80 00 80 00 20 00 20 CC 33 C3 3C DMT32240F028-06WN: It takes 1.6 ms to execute this example command. (typically 1.4~2.1ms, depending on JPEG file size).

3 Download Mode

(1) Enter Download Mode

Transmit AA 3F 5A A5 BODE_SET (4 bytes) CC 33 C3 3C via serial port to enter download mode.

BODE_SET configures the serial baud rate for download. For example, 0x000E1000 corresponds to 921600 bps.

(2) Download Mode Command Format

0x5AA5 (Frame header) + LEN_H:L (Command and data length) + CMD (Command) + DATAs (Data) + CRC_H:L (CRC checksum)

LEN_H:L indicates the total byte length of CMD + DATAs, excluding CRC. Maximum value: 0x1010.

CRC_H:L is the 16-bit MODBUS-style CRC checksum of CMD and DATAs.

(3) Download Mode Command Set

CMD (Command)	Function	DATAs
0x50	Handshake	Tx: None Rx: 0x4F 0x4B
0x52	Clear Screen	Tx: COLOR_R:G:B Rx: 0x4F 0x4B
0x53	Text Display	Tx: COLOR_R:G:B + B_COLOR_R:G:B + (x, y) + Strings + 0x00 Rx: 0x4F 0x4B COLOR_R:G:B stands for character color, and B_COLOR_R:G:B stands for background color. It supports 8 × 12 dot matrix text display, only for ASCII characters ranging from 0x20 to 0x5F.
0x55	Data Download	Tx: Start Address (ADR_H:M_H:M_L:L) + Data (maximum 4KB) Rx: Start Address + 0xFF (OK) / 0x00 (Error) T5S0 will respond only after data is written successfully.

CMD (Command)	Function	DATAs
		The start address must be 4KB-aligned (the lower 12 bits are 0), and each erase operation is 4KB. If the written data is less than 4KB, T5S0 will pad the remaining space with 0x00.
0x5A	4KB Block CRC Check	Tx: Start Address (ADR_H:M_H:M_L:L) Rx: Start Address + CRC_H:L The start address must be 4KB-aligned (the lower 12 bits are 0). CRC check cannot be performed on T5S0 code. During OTA upgrade, CRC check will be executed on Flash data first. Data download will only start when CRC mismatch is detected, so as to improve download speed.
0x5E	Exit Download	Tx: None Rx: 0x4F 0x4B After responding, T5S0 will exit download mode and restore the original serial port settings.
0x5F	Reset Reboot	Tx: None Rx: 0x4F 0x4B T5S0 will reset and reboot after responding.

(4) Flash Address Mapping Table

Start Address	Data Location	Space Size	Description
0xFF F0 00 00	On-chip Flash	64KB	GUI code, T5S0_UI*.BIN
0xFF F1 00 00	On-chip Flash	64KB	TPS04 code, T5S0_OS*.BIN
0xFF F2 00 00	On-chip Flash	64KB	System reserved, write prohibited.
0xFF F3 00 00	On-chip Flash	32KB	On-chip 32KB Flash database, T5S0*.LIB.
0xFF F3 80 00	On-chip Flash	4KB	CFG file, T5S0*.CFG.
0xFF F3 90 00	On-chip Flash	16KB	System reserved, write prohibited.
0xFF F3 C0 00	On-chip Flash	12KB	INI file, T5S0*.INI.
0x00 00 00 00	Off-chip Flash	Max 16MB	Font library files, numeric ID (0-255) *.BIN or *.ICL. File start address = File ID * 0x01: 0000. For example, the start address of File No.12 is 0x000C: 0000.

(5) PGT05F6 Programming Tool

The PGT05F6 is a programming tool for the 06-series COF screens. It is powered via a 5V USB interface and supports downloading at 2.46 Mbps. The operating steps are as follows:

1. Insert a TF card containing programming files into the PGT05F6. (Files must be placed under the 'DWIN_SET' folder in the root directory; the TF card shall be formatted as FAT32 with 4KB sectors.)
2. Power on the PGT05F6 and wait for the red LED to light up. If the red LED stays off, the TF card is not detected.
3. Connect the COF screen to be programmed. Press the button to start programming; the red LED will turn off and programming begins.

Once programming completes, the PGT05F6 will automatically power-cycle the COF screen, which then displays the boot configuration interface.

4. Press the button to finish programming. The PGT05F6 cuts power to the COF screen, the red LED lights up, and you may remove the programmed COF screen.
5. Repeat steps 3 - 4 to program additional COF screens.

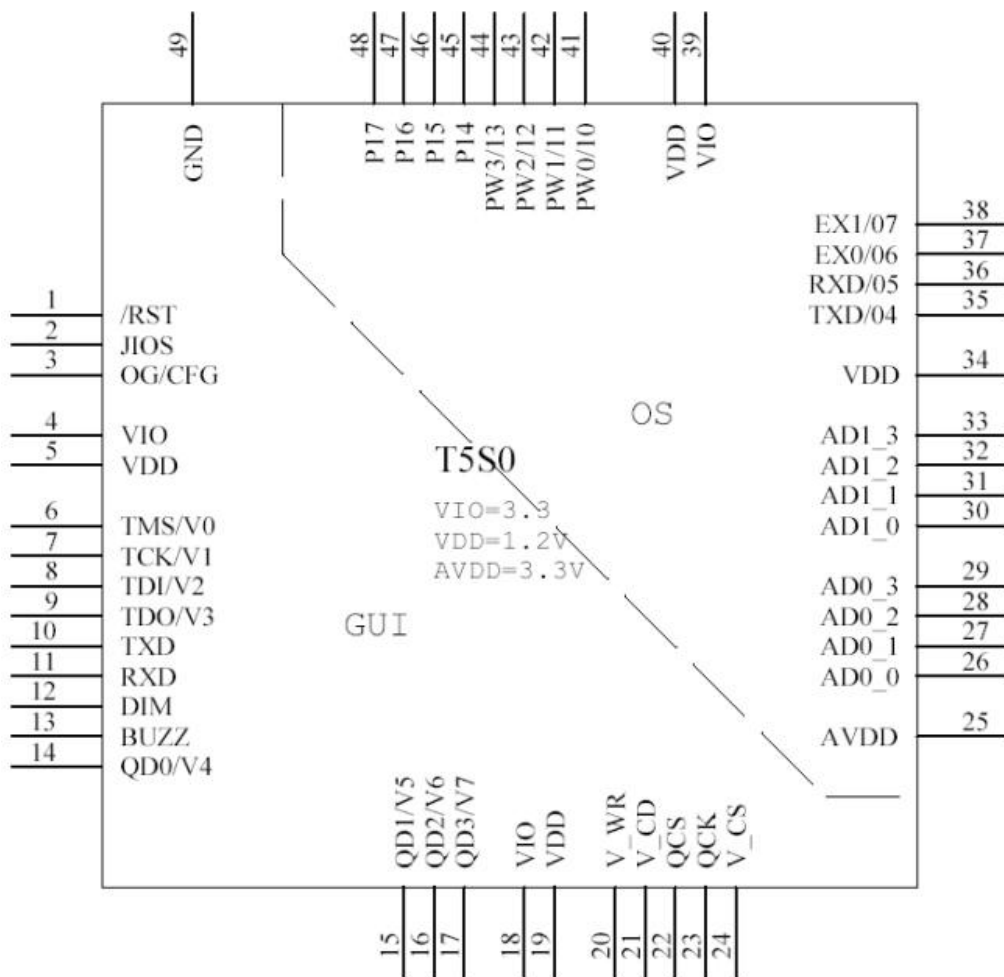
The average download/update speed of the PGT05F6 is around 150 KB/S.

4 Hardware Configuration File Format (*.CFG)

Type	Address	Length	Definition	Description
Configuration Identification	0x00	4	0x54 0x35 0x53 0x30	Fixed content.
Reserved	0x04	12	Reserved	Write 0x00.
System Configuration	0x10	2	System Configuration Enable	0x5AA5 indicates that the current configuration modification is valid.
	0x12	1	System Configuration	Bit7: Power-on display setting 0=Display boot image; 1=Black screen clear. Bit6: Serial port CRC check switch 0=Disabled; 1=Enabled. Bit5: OS kernel switch 0=Disabled. Disable it to reduce power consumption if the OS kernel is not used for secondary development. 1=Enabled. Bit4~Bit 2: Undefined, write 0. Bit1~Bit 0: Power-on display orientation setting 0x00 (00) =0 degree, no rotation. 0x01 (01) =90-degree rotation. 0x02 (10) =180 degrees, view flip. 0x03 (11) =270-degree rotation. Factory default: 0x00 (Display boot image on power-up; CRC disabled; OS kernel disabled, no rotation).
	0x13	4	UART Baud Rate Setting	Baud rate value, e.g. 115200bps=0x00 01 C2 00. The baud rate reference clock is 7.3728Mbps. If the frequency division coefficient 7372800/baud rate value is not an integer, the

Type	Address	Length	Definition	Description
				actual baud rate will have an error due to rounding of the frequency division coefficient. Factory default: 0x00 01 C2 00 (115200bps).
	0x17	1	Power-on Backlight Brightness Setting	Range: 0x00~0xFF. 0x00 means backlight off, 0xFF is maximum backlight brightness. Factory default: 0xFF.
	0x18	8	Reserved	Write 0x00.
Display Configuration	0x20	2	Display Configuration Enable	0x5AA5 indicates the current configuration modification is valid. Pre-configured at factory, users are not allowed to modify. Write 0x0000.
	0x22	2	Display Horizontal Resolution	Set according to the actual physical resolution of the display, rotation configuration is not considered.
	0x24	2	Display Vertical Resolution	
	0x26	4	Reserved	Write 0x00.
Boot Image Configuration	0x2A	2	Boot Image Configuration Enable	0x5AA5 indicates the current configuration modification is valid.
	0x2C	2	Image ICL File Address	0x0000~0x00FF. Factory default: 0x0028.
	0x2E	2	Image ID	0x0000~0xFFFF. Factory default: 0x0000.
Reserved	0x30	208	Reserved	Write 0x00.

5 T5S0 Chip Package Definition (4×4mm QFN48 Package)



Pin#	Definition	Description	Different LCD Panel Connections			Pin#	Definition	Description
			SPI	QSPI	8080			
1	/RST	Reset input, active low reset.				25	AVDD	3.3V; Low ripple required if AD is used.
2	JIOS	PIN#6-PIN#9 JTAG/IO selection: 0=JTAG, 1=IO (LCD interface).				26	AD0_0	ADC0, 4-channel AD. Input impedance: 10kΩ.
3	OG/CFG	JTAG mode: 0=JTAG connected to GUI core, 1=OS core. IO mode: 0=User mode, 1=Configuration mode.				27	AD0_1	
4	VIO	3.2V				28	AD0_2	
5	VDD	1.2V				29	AD0_3	

6	TMS/V0	JTAG Interface: Also used as LCD data interface.		D0	D0	30	AD1_0	ADC1, 4-channel AD. Input impedance: 10k Ω .
7	TCK/V1			D1	D1	31	AD1_1	
8	TDI/V2			D2	D2	32	AD1_2	
9	TDO/V2		SDA	D3	D3	33	AD1_3	
10	TXD	User UART TXD (T5S0 OUT).				34	VDD	1.2V
11	RXD	User UART RXD (T5S0 IN).				35	TXD/0.4	UART TXD, multiplexed with P0.4 IO.
12	DIM	Backlight brightness adjustment PWM output.				36	RXD/0.5	UART RXD, multiplexed with P0.5 IO.
13	BUZZ	Buzzer or audio signal output.				37	EX0/0.6	P0.6, External Interrupt 0 input.
14	QD0/V4	Data signal for external QSPI NOR. When using parallel LCD, it also serves as the high 4-bit data signal.			D4	38	EX1/0.7	P0.7, External Interrupt 1 input.
15	QD1/V5				D5	39	VIO	3.3V
16	QD2/V6				D6	40	VDD	1.2V
17	QD3/V7				D7	41	PWM0/1.0	4-channel PWM multiplexed IO.
18	VIO	3.3V				42	PWM1/1.1	
19	VDD	1.2V				43	PWM2/1.2	
20	V_WR	LCD interface signal, write.	SCK	SCK	WR	44	PWM3/1.3	
21	V_CD	LCD interface signal, instruction/data	C/D	C/D	C/D	45	P1.4	
22	QCS	CS signal for external QSPI NOR.				46	P1.5	
23	QCK	CLK signal for external QSPI NOR.				47	P1.6	
24	V_CS	LCD interface signal, chip select.	CS	CS	CS	48	P1.7	
49	GND	The ground pad is on the bottom side of the chip.						

It is recommended to use the 8080 interface to connect the LCD screen during customer design (the RD signal of the LCD is fixed at high level).

6 OS CPU Function Module Programming Description

The OS CPU of T5S0 adopts the widely used and field-proven 8051 core for industrial applications with a long mass-production history, running at a main frequency of 236 MHz (internal oscillator, factory-calibrated accuracy $\pm 2\%$ across the full operating temperature range of $-40 / +85^{\circ}\text{C}$).

6.1 Initialization Configuration

After the OS CPU core is powered on, it must initialize the special function registers (SFR) in the chip.

SFR Name	Address	Initial Configuration Value	Description
CKCON	0x8E	0x00	CPU operates in 1T mode.
T2CON	0xC8	0x70	Configure the extended interrupt system and set Timer T2 to Autoload mode.
DPC	0x93	0x00 or 0x01	DPTR update mode after MOVX instruction execution. For C51 development, this must be set to 0x00. 0x00: No change. 0x01: DPTR=DPTR+1. 0x03: DPTR=DPTR-1.
PAGESEL	0x94	0x00 or 0x01	The OS CPU features 64KB RAM for code execution and data access via MOVX instructions. It is divided into two 32KB pages with corresponding page addresses of 0x00 - 0x01. Page 0 is exclusively for code storage, mapped to DPTR addresses 0x0000 - 0x7FFF. Page 1 can be switched by PAGESEL (code space, read via MOVC instruction) or D_PAGESEL (data space, read/write via MOVX instruction), and is mapped to the address range 0x8000~0xFFFF for read and write operations.
D_PAGESEL	0x95	0x01	
MUX_SEL	0xC9	0x40 or as required by the application	Bit 7: Reserved, write 0. Bit 6: 1=UART interface routed to P0.4 and P0.5; 0=UART interface not routed, pins function as GPIO. Bit 5~Bit 2: Reserved, write 0. Bit 1: WDT control. 1=Enable; 0=Disable. Bit 0: WDT feed. 1=Feed watchdog once (WDT counter reset to zero).
MUX_SEL1	0xE9	0x40 or as required by the application	Bit7~Bit4: Undefined, write 0. Bit3: 1=PWM3 interface routed to P1.3;

			0=PWM3 interface not routed, pin functions as IO. Bit2: 1=PWM2 interface routed to P1.2; 0=PWM2 interface not routed, pin functions as IO. Bit1: 1=PWM1 interface routed to P1.1; 0=PWM1 interface not routed, pin functions as IO. Bit0: 1=PWM0 interface routed to P1.0; 0=PWM0 interface not routed, pin functions as IO.
P0MDOUT	0xB7	As required by the application	P0 port output configuration (IO input reading is always valid; when configured as output, the IO status can still be read). Bit7: 0=P0.7 output disabled; 1=P0.7 output enabled (push-pull output). Bit6: 0=P0.6 output disabled; 1=P0.6 output enabled (push-pull output). Bit5: 0=P0.5 output disabled; 1=P0.5 output enabled (push-pull output). Bit4: 0=P0.4 output disabled; 1=P0.4 output enabled (push-pull output). Bits3~Bit0: Reserved, write 0.
P1MDOUT	0xBC	As required by the application	P0 port output configuration (IO input reading is always valid; when configured as output, the IO status can still be read).
PORTDRV	0xF9	0x01 or as required by the application	IO port output mode drive strength configuration. Only the least significant 3 bits are valid: 0x00=4mA 0x01=8mA 0x02=16mA 0x03=32mA 0x04=48mA 0x05=64mA 0x06=80mA 0x07=100mA
RAMMODE	0xF8	0x00	Variable memory access interface control.

6.2 Memory

The 8051 core of the OS CPU can access 6 different types of memory, as shown in the table below.

Memory Type	Size	Address Space	Access Method
Code Memory	64KBytes	0x0000-0xFFFF	PAGESEL switches code page space, read only via MOVC instruction.
Data Register	256Bytes	0x00-0xFF	Same as standard 8051.

SFR Register	128Bytes	0x80-0xFF	DWIN can provide user SFR definition .INC or .H header files.
Extended SFR Registers	78Bytes	0x00-0x4D	Accessed via EXADR, EXDATA register interfaces.
Data Memory	32KBytes	0x8000-0xFFFF	Set D_PAGESEL=0x01, access using MOVX instruction.
Variable Memory	4KBytes	0x01:2C00-0x01:2FFF	Accessed via variable memory interface.

6.2.1 Code Memory (Maximum 64KBytes)

The functional partition and definition of the code memory space are shown below.

Address	Definition	Description
0x0000	Reset_PC	Program start address after reset
0x0003	EX0_ISR_PC	External interrupt 0 program entry.
0x000B	T0_ISR_PC	Timer0 interrupt program entry.
0x0013	EX1_ISR_PC	External interrupt 1 program entry.
0x001B	T1_ISR_PC	Timer1 interrupt program entry.
0x0023	UART2_ISR_PC	UART2 TX/RX interrupt program entry.
0x002B	T2_ISR_PC	Timer2 interrupt program entry.
0x008B	PWM0_ISR_PC	PWM0 reload interrupt program entry.
0x0093	PWM1_ISR_PC	PWM1 reload interrupt program entry.
0x009B	PWM2_ISR_PC	PWM2 reload interrupt program entry.
0x00A3	PWM3_ISR_PC	PWM3 reload interrupt program entry.
0x00AB	AD_ISR_PC	AD data conversion interrupt program entry.
0x00F8	JTAG interface enable	0xFFFF allows JTAG interface connection for emulation and debugging; other values disable this function.
0x00FA	"DWINT5"	Code identification. Invalid values will halt the OS CPU.
0x0100	Application code start	

OS CPU code is stored in the on-chip Flash. After power-on reset, it is loaded into RAM by system hardware for execution.

OS CPU code can only be written into the on-chip Flash via the GUI CPU.

6.2.2 Variable Memory (4KBytes)

The variable memory is dual-port RAM, used for high-speed data exchange between two CPU cores. Its address range is 0x012000-0x012FFF. Out-of-bound writes may lead to abnormal display or other unpredictable failures. Among this range, 0x000000-0x012BFF is display memory, and addresses after 0x013000 belong to GUI core variable memory. Each address corresponds to

4Bytes of data. Access to variable memory uses the SFR register interface shown in the table below:

SFR Name	Address	Description
RAMMODE	0xF8	Variable memory access interface control, bit-addressable : Bit7: Write 1 to request occupation of variable memory for read/write operation; must be cleared when not in use. Bit6: APP_EN. Write 1 to trigger one read/write operation; cleared by hardware after execution. Bit5: APP_RW. 1=read variable memory; 0=write variable memory. Bit4: APP_ACK. Hardware response to the 8051 request for variable memory occupation: 1=OK, 0=BUSY (wait required). Bit3~Bit0: Corresponding DATA3:DATA0 write enable. 1=write the respective byte; 0=skip writing the respective byte.
ADR_H	0xF1	Variable memory high 8-bit address, fixed at 0x01.
ADR_M	0xF2	Variable memory middle 8-bit address, fixed at 0x2D.
ADR_L	0xF3	Variable memory low 8-bit address, A7:A0, ranging from 0x00 to 0xFF.
ADR_INC	0xF4	Increment for automatic address increment after variable memory read/write. After read/write, ADR_H:M:L=previous ADR_H:M:L + ADR_INC.
DATA3	0xFA	Variable data interface, write selection corresponding to RAMMODE.3.
DATA2	0xFB	Variable data interface, write selection corresponding to RAMMODE.2.
DATA1	0xFC	Variable data interface, write selection corresponding to RAMMODE.1.
DATA0	0xFD	Variable data interface, write selection corresponding to RAMMODE.0.

Variable memory must be read and written following the procedure below. (If used within an interrupt, interrupts must be disabled during main program read/write operations; nesting is not allowed.)

- (1) Configure the address and address increment;
- (2) Set RAMMODE=0x8F (write) or 0xAF (read). Check RAMMODE.4=1 to confirm read/write control is acquired;
- (3) Read or write data, then set RAMMODE=0x00 after completion.

Application example: Read/Write 2 double words starting at address 0x012D00

```

MOV  ADR_H, #01H      ;Configure variable memory address
MOV  ADR_M, #2DH
MOV  ADR_L, #00H
MOV  ADR_INC, #01H    ;Configure address increment
MOV  RAMMODE, #0AFH   ;Enable read mode
JNB  APP_ACK, $        ;Wait for acknowledgement
MOV  R0, #TEST_BUF    ;Demo read operation
MOV  R1, #2

```

```

RDVP: SETB  APP_EN      ;Trigger one read operation

```

```

JB   APP_EN, $

```

```

MOV  @R0, DATA3
INC  R0
MOV  @R0, DATA2
INC  R0
MOV  @R0, DATA1
INC  R0
MOV  @R0, DATA0
INC  R0
DJNZ R1, RDVP
CLR  APP_RW          ;Write mode, demo write operation
MOV  ADR_L, #00H     ;Reset address to 0x01:2D00
MOV  R0, #TEST_BUF
MOV  R1, #2
WRVP: MOV  DATA3, @R0
INC  R0
MOV  DATA2, @R0
INC  R0
MOV  DATA1, @R0
INC  R0
MOV  DATA0, @R0
SETB APP_EN          ;Trigger one write operation
JB   APP_EN, $
INC  R0
DJNZ R1, WRVP
MOV  RAMMODE, #00H    ;Variable memory read/write completed

```

6.2.3 Data Memory (Maximum 32KBytes)

The OS CPU of T5S0 has a maximum of one 32KBytes RAM page block serving as data memory, corresponding to the address range 0x80000-0xFFFF. Relevant interface SFRs are described below.

SFR Name	Address	Description
D_PAGESEL	0x95	Page block select register, fixed at 0x01.
DPC	0x93	Configures the change mode of DPTR after MOVX instructions with DPTR. DPC=0x00: DPTR stays unchanged after MOVX operation, and it must be set to 0x00 for C51 development. DPC=0x01: DPTR=DPTR+1 after MOVX operation. DPC=0x03: DPTR=DPTR-1 after MOVX operation.

DPH	0x83	DPTR data pointer.
DPL	0x82	

The address space 0x0000-0x7FFF must not be read or written via MOVX instructions; otherwise abnormal code operation may be triggered.

The MOVX instruction of T5S0 costs 3 instruction cycles. DPC supports DPTR auto-increment or auto-decrement configuration, enabling T5S0 to access data memory much faster than the standard 8051, especially for reverse-order memory read and write scenarios.

Application example:

```
MOV    DPC, #01H      ;DPTR++
MOV    DPTR, #8000H
MOVX   A, @DPTR       ;A= 0x8000
MOVX   A, @DPTR       ;A= 0x8001, DPTR becomes 0x8002 after read
```

6.2.4 Extended SFR Registers

Extended SFR registers are read and written via the EXADR and EXDATA register interfaces.

SFR Name	Address	Description
EXADR	0xFE	The address automatically increments by 1 after each read or write operation to point to the next SFR.
EXDATA	0xFF	Data interface for extended SFR registers.

If extended SFR registers are used in interrupt applications, interrupts must be disabled when the main program reads or writes extended SFR registers. Nested operations are not allowed.

Definitions of extended SFR registers are described below:

Category	Address	Length	Definition	Description
MDU	0x00	1	A7	Register group for MDU arithmetic acceleration. Byte 7 is the most significant byte and byte 0 is the least significant byte.
	0x00-0x07	6	A6-A0	
	0x08	8	B7: B0	
	0x10	8	C7:C0	
ADC	0x18	16	AD0-AD7	8-channel AD values, 2 bytes per channel.
	0x48	1	ADC_PGA	
	0x49	5	ADC_CFG0-4	
WDT	0x30	4	WDT_Time_Set	WDT_Time_Set. Description: WDT counter setting based on CPU clock. T5S0 will be reset when the WDT counter exceeds the set value.
PWM	0x34	1	PWM0_CLK_DIV	PWM0 operating frequency=1416MHz / PWM0_CLK_DIV.
	0x35	2	PWM0_TH: L	PWM0 count upper limit setting. PWM0 carrier frequency=PWM0 operating frequency/(PWM0_TH:L+1).
	0x37	2	PWM0_H: L	High-level width value of PWM0 output.
	0x39	5	PWM1 configuration value	

	0x3E	5	PWM2 configuration value	
	0x43	5	PWM3 configuration value	

6.3 Multiplication/Division Unit (MDU)

Due to the limited computing capability of the 8051 core, T5S0 integrates a hardware integer arithmetic unit (MDU) to boost computation performance. For this integer arithmetic unit, the division instruction takes up to 32T (typically 8T), while all other instructions complete within 2T.

Definitions of relevant control SFRs are listed below:

SFR Name	Address	Description
MAC_CN	0xE5	MAC hardware integer multiply-accumulator control register, defined as follows: Bit7: MAC enable. Write 1 to trigger one calculation; hardware clears this bit after computation completes. Bit6: MAC mode. 1 = multiply-accumulate mode: $C=A \times B+C$; 0=multiplier mode: $C=A \times B$. Bit5: Write 0. Bit4: 1=64-bit MAC; 0=32-bit MAC (A3:0/B3:0/C7:0; note that C remains 64-bit). Bit3: 1=signed number; 0=unsigned number. Bit2~Bit0: Write 0. Register groups A, B and C correspond to the A, B, C register groups in extended SFRs.
DIV_CN	0xE6	DIV hardware integer divider control register (division C/A ; quotient stored in A, remainder stored in B), defined as follows: Bit7: DIV enable. Write 1 to trigger one calculation; hardware clears this bit after computation completes. Bit6: DIV mode. 1=round to nearest; 0=no rounding. Bit5~Bit4: Undefined; write 0. Bit3: 1=signed number; 0=unsigned number. Bit2~Bit0: Write 0. Register groups A, B and C correspond to the A, B, C register groups in extended SFRs.

Application example: 32-bit integer MAC calculation of $0x1234 \times 0x5678-0x2000$

```
MOV  EXADR, #04H      ;Write A3: A0 = 0x00 00 12 34
MOV  EXDATA, #00H
MOV  EXDATA, #00H
MOV  EXDATA, #12H
MOV  EXDATA, #34H
MOV  EXADR, #0CH      ;Write B3: B0 = 0x00 00 56 78
MOV  EXDATA, #00H
MOV  EXDATA, #00H
```

```
MOV  EXDATA, #56H
MOV  EXDATA, #78H
MOV  EXADR, #10H      ;Write C7: C0=0xFF FF FF FF FF E0 00 (-0x2000)
MOV  EXDATA, #0FFH
MOV  EXDATA, #0FFH
MOV  EXDATA, #0FFH
MOV  EXDATA, #0FFH
MOV  EXDATA, #0FFH
MOV  EXDATA, #0FFH
MOV  EXDATA, #0FFH
MOV  EXDATA, #0E0H
MOV  EXDATA, #00H
MOV  MAC_CN, #0C8H    ;32-bit integer MAC, trigger one computation
NOP
MOV  EXADR, #10H      ;Read result: 00 00 00 00 06 25 E0 60
MOV  R7, EXDATA
MOV  R6, EXDATA
MOV  R5, EXDATA
MOV  R4, EXDATA
MOV  R3, EXDATA
MOV  R2, EXDATA
MOV  R1, EXDATA
MOV  R0, EXDATA
MOV  MAC_CN, #00H
```

6.4 Timer

The OS CPU of T5S0 has three timers T0/T1/T2. T0 and T1 are consistent with standard 8051, and T2 can only operate in 16-bit Autoreload mode.

The clock of T0 and T1 is 1/12 of the CPU main frequency, and the clock of T2 can be configured as 1/12 or 1/24 of the CPU main frequency.

Timer-related SFRs are described as follows:

SFR Name	Address	Description
TCON	0x88	T0 and T1 control register, same as standard 8051 and bit-addressable . Bit7=TF1, Bit6=TR1, Bit5=TF0, Bit4=TR0, Bit3=IE1, Bit2=IT1, Bit1=IE0, Bit0=IT0. IT1 and IT0 are external interrupt trigger mode selection bits: 0 for low-level trigger, 1 for falling-edge trigger.
TM0D	0x89	Mode selector for T0 and T1, same as standard 8051.
TH0	0x8C	
TL0	0x8A	
TH1	0x8D	
TL1	0x8B	
T2CON	0xC8	T2 control register, bit-addressable . Bit7: clock divider selection, 0=CPU main frequency/12, 1=CPU main frequency/24. Bit6~Bit4: must be written as 1. Bit3~Bit1: must be written as 0. Bit0: TR2, 1=T2 running, 0=T2 closed.
TH2	0xCD	T2 running value. TH2=CRCH and TL2=CRCL will be auto-reloaded when counting overflows.
TL2	0xCC	
TRL_2H	0xCB	T2 reload value= $65536 - T2 \text{ timer interval } (\mu s) \times T2 \text{ clock frequency (MHz)}$.
TRL_2L	0xCA	

Settings related to timer interrupts are as follows:

Interrupt Type	Program Entry Address	Trigger Flag	Interrupt Enable Control	Remark
T0 interrupt	0x000B	TF0 (TCON.5)	IEN0.1	TF0 is automatically cleared upon interrupt response.
T1 interrupt	0x001B	TF1 (TCON.7)	IEN0.3	TF1 is automatically cleared upon interrupt response.
T2 interrupt	0x002B	TF2 (IRCON.6)	IEN0.5	Program entry address 0x002B, trigger flag TF2 (IRCON.6), interrupt enable control IEN0.5. TF2 must be cleared by software

				after interrupt response; otherwise the interrupt will be triggered repeatedly.
--	--	--	--	---

Application example: Configure T2 to generate 1ms interrupt and output a 500Hz square wave at P1.0.

```
ORG    002BH           ;Interrupt entry address of T2
LJMP   T2INT
```

```
T2INT: CLR TF2           ;T2 interrupt service routine
      CPL P1.0
      RETI
```

```
;Initialize T2 related SFRs
MOV CRCH, #HIGH(45869) ;1ms timer
MOV CRCL, #LOW(45869)
MOV T2CON, #71H        ;TR2=1, T2 clock=CPU main frequency/12
ORL IEN0, #20H         ;ET2=1, enable T2 interrupt
```

6.5 Watchdog Timer (WDT)

The Special Function Registers (SFRs) for Watchdog Timer control are listed in the table below:

SFR Name	Address	Description
MUX_SEL	0xC9	Bit1: WDT control. 1=Enable, 0=Disable. Bit0: WDT watchdog feed. Write 1 to feed the watchdog once (WDT counter resets to zero).

The WDT overflow time is stored at extended SFR address 0x030. WDT reset time = Set value / CPU main frequency (Hz), unit: second.

Reference code for WDT operation is shown below:

```
ANL    MUX_SEL, #0FDH ;WDT must be disabled before setting overflow time
MOV    EXADR, #30H    ;Configure WDT reset time to 1s at 236 MHz main frequency
=236000000 (0x0E 11 13 00)
MOV    EXDATA, #0EH
MOV    EXDATA, #11H
MOV    EXDATA, #13H
MOV    EXDATA, #00H
ORL    MUX_SEL, #02H  ;Enable WDT. Once enabled, the watchdog must be fed
before WDT overflow to prevent system reset.
```

ORL MUX_SEL, #01H ;WDT reset (feed watchdog)

6.6 Pulse Width Modulation Module (PWM)

The Special Function Registers (SFRs) for Watchdog Timer control are listed in the table below:

1. SFR registers related to PWM control

SFR Name	Address	Description
MUX_SEL1	0xE9	Bit3: 1= PWM3 interface routed to P1.3; 0=PWM3 interface not routed, P1.3 acts as IO. Bit2: 1=PWM2 interface routed to P1.2; 0=PWM2 interface not routed, P1.2 acts as IO. Bit1: 1=PWM1 interface routed to P1.1; 0=PWM1 interface not routed, P1.1 acts as IO. Bit0: 1=PWM0 interface routed to P1.0; 0=PWM0 interface not routed, P1.0 acts as IO.
PWM0_CN	0xEB	Bit7(W): PWM0_EN. 1=Enable PWM0, 0=Disable PWM0. Bit6(R/W): PWM0_IF, PWM0 interrupt flag. Set by hardware, cleared by CPU. Bit5(R/W): PWM configuration update bit. Writing 1 updates extended SFR registers 0x034~0x036, cleared by hardware after processing. Bit4~Bit0: Reserved, undefined.
PWM1_CN	0xEC	Bit definition is the same as PWM0_CN.
PWM2_CN	0xED	Bit definition is the same as PWM0_CN.
PWM3_CN	0xEE	Bit definition is the same as PWM0_CN.
P1MDOUT	0xBC	P1 port output configuration. IO input reading is always valid. When configured as output, the IO status can still be read. Bit3: 0=P1.3 output disabled; 1=P1.3 output enabled (push-pull output). Bit2: 0=P1.2 output disabled; 1=P1.2 output enabled (push-pull output). Bit1: 0=P1.1 output disabled; 1=P1.1 output enabled (push-pull output). Bit0: 0=P1.0 output disabled; 1=P1.0 output enabled (push-pull output).

2. Extended SFR registers related to PWM control

Address	Length	Definition	Description
0x34	1	PWM_CLK_DIV	PWM0_CLK_DIV Description: PWM0 operating frequency=1416MHz / PWM0_CLK_DIV.
0x35	2	PWM_TH:L	PWM0 count upper limit setting. PWM0 carrier frequency= PWM0 operating frequency / (PWM0_TH:L + 1).
0x37	2	PWM_H:L	High-level width value of PWM0 output.
0x39	5	PWM1 Configuration	
0x3E	5	PWM2 Configuration	
0x43	5	PWM3 Configuration	

3. Extended SFR registers related to PWM control

Interrupt Type	Program Entry Address	Trigger Flag	Interrupt Enable Control	Remark
PWM0 interrupt	0x008B	PWM0_CN.6	IEN2.1	PWM0_CN.6 needs to be cleared by software after the interrupt is acknowledged.
PWM1 interrupt	0x0093	PWM1_CN.6	IEN2.2	PWM1_CN.6 needs to be cleared by software after the interrupt is acknowledged.
PWM2 interrupt	0x009B	PWM2_CN.6	IEN2.3	PWM2_CN.6 needs to be cleared by software after the interrupt is acknowledged.
PWM3 interrupt	0x00A3	PWM3_CN.6	IEN2.4	PWM3_CN.6 needs to be cleared by software after the interrupt is acknowledged.

Application example: Configure PWM0 as 8-bit PWM with approx. 300KHz frequency and adjust PWM output duty cycle inside PWM interrupt.

;PWM0 Initialization

MOV EXADR, #34H

MOV EXDATA, #18

;PWM0 frequency = $1416\text{MHz}/(18 \times 256) = 307\text{KHz}$

MOV EXDATA, #00H

;Count upper limit

MOV EXDATA, #255

MOV EXDATA, #00H

;Initialize output high level to 0%

MOV EXDATA, #00H

MOV PWM0_CN, #0A0H

;Configure and enable PWM0 once

ORL P1MDOUT, #01H

;P1.0 set as output

ORL MUX_SEL1, #01H

;Set P1.0 as PWM0 output

ORL IEN2, #02H

;Enable PWM0 interrupt

;PWM0 Interrupt Service Routine (Use the yellow-highlighted codes above inside ISR if real-time frequency adjustment is required)

MOV EXADR, #37H ;Extended SFR used in interrupt routine, interrupts must be disabled when accessing extended SFR in main program.

MOV EXDATA, #00H

MOV EXDATA, PWM0_DUTY

ANL PWM0_CN, #0BFH ;Clear PWM0 interrupt flag

6.7 I/O Ports

T5S0's OS CPU features one 8-bit parallel port (P1) and one 4-bit quasi-parallel port (P0.4 - P0.7), providing a total of 12 I/O pins.

Input mode is always enabled for all I/O pins; inputs are floating with no internal pull-up or pull-down resistors.

When an I/O pin is used as an output, the output control must be enabled, and the output drive strength is configurable. Since I/O pins default to input mode during power-on reset, external pull-up or pull-down resistors are required for output applications to guarantee stable, defined output levels during power-up and prevent unintended floating behavior.

P0.6 serves as External Interrupt 0 input, and P0.7 serves as External Interrupt 1 input. They can be configured via IT0 and IT1 for level trigger (0) or falling-edge trigger (1).

Except for output enable switches and peripheral multiplex power-on initialization, subsequent I/O operation is compatible with standard 8051.

I/O-related SFRs are listed below:

SFR Name	Address	Description
P0	0x80	Bit-addressable, same as standard 8051.
P1	0x90	Bit-addressable, same as standard 8051.
P0MDOUT	0xB7	Bit7: 0=P0.7 output disabled; 1=P0.7 output enabled (push-pull output). Bit6: 0=P0.6 output disabled; 1= P0.6 output enabled (push-pull output). Bit5: 0=P0.5 output disabled; 1=P0.5 output enabled (push-pull output). Bit4: 0=P0.4 output disabled; 1= P0.4 output enabled (push-pull output). Bit3~Bit0: Reserved, write 0.
P1MDOUT	0xBC	P1 port output configuration.
MUX_SEL	0xC9	Bit7: Reserved, write 0. Bit6: 1=UART routed to P0.4, P0.5; 0=UART not routed, pins function as IO. Bit5~Bit2: Reserved, write 0. Bit1: WDT control. 1=Enable; 0=Disable. Bit0: WDT feed. 1= Feed watchdog once (WDT counter cleared).
MUX_SEL1	0xE9	Bit7: ADC conversion complete interrupt flag, set by hardware, cleared by CPU (ANL MUX_SEL1,#7FH). Bit6~Bit4: Undefined, write 0. Bit3: 1=PWM3 routed to P1.3; 0=PWM3 not routed, pin functions as IO. Bit2: 1=PWM2 routed to P1.2; 0=PWM2 not routed, pin functions as IO.

		Bit1: 1=PWM1 routed to P1.1; 0=PWM1 not routed, pin functions as IO. Bit0: 1=PWM0 routed to P1.0; 0=PWM0 not routed, pin functions as IO.
PORTDRV	0xF9	I/O output drive strength configuration. Only the lower 3 bits are valid. 0x00=4mA, 0x01=8mA, 0x02=16mA, 0x03=32mA, 0x04=48mA, 0x05=64mA, 0x06=80mA, 0x07=100mA.

I/O port external interrupt related configurations are as followed:

Interrupt Type	Program Entry Address	Trigger Flag	Interrupt Enable Control	Remark
EX0 interrupt	0x0003	IE0 (TCON.1)	IEN0.0	IE0 is automatically cleared upon interrupt acknowledgment. Corresponding input pin is P0.6. IT0 (TCON.0)=0: low-level triggered interrupt; IT0=1: falling-edge triggered interrupt.
EX1 interrupt	0x0013	IE1 (TCON.3)	IEN0.2	IE1 is automatically cleared upon interrupt acknowledgment. Corresponding input pin is P0.7. IT1 (TCON.2)=0: low-level triggered interrupt; IT1=1: falling-edge triggered interrupt.

6.8 AD Conversion

The AD contains two independent 4-channel AD converters. Related SFRs are listed in the table below.

SFR Name	Address	Description
AD_CLK_L	0x8F	AD_CLK_H:L=16.09MHz / AD sampling rate. The maximum AD sampling rate is 1MSPS and the minimum is 2KSPS. Example: set per-channel AD sampling rate to 64KSPS, then AD_CLK_H:L= 16090/64=252 (0x00FC).
AD_CLK_H	0x91	
ADC_SET	0xAD	Bit7: ADC_EN. 1=Enable, 0=Disable. Bit 6: ADC0_IF. Interrupt flag at end of one conversion for ADC0 (AD00-AD03). Set by hardware, cleared by software. Bit 5: ADC1_IF. Interrupt flag at end of one conversion for ADC1 (AD10-

		AD13). Set by hardware, cleared by software. Bit4~Bit0: Write 0.
ADC_POL	0xAE	0x0F=ADC00-ADC03, 4 ADC channels (CH0-CH3) enabled. 0xF0=ADC10-ADC13, 4 ADC channels (CH4-CH7) enabled. 0xFF=ADC00-ADC03 and ADC10-ADC13, all 8 ADC channels (CH0-CH7) enabled.

Extended SFRs related to AD conversion are shown below.

Address	Length	Definition	Description
0x18	16	AD_CH0-AD_CH7	8-channel AD conversion results. 2 bytes per channel, high byte first. 12-bit resolution, AVDD as reference voltage.
0x48	1	ADC_PGA	Configurable from 0x00 to 0x09, corresponding to internal PGA gain 1-10. Recommended setting: 0x00 (no amplification).
0x49	1	ADC_CFG0	Configure to 0x42.
0x4A	1	ADC_CFG1	Configure to 0x00.
0x4B	1	ADC_CFG2	Configure to 0x05.
0x4C	1	ADC_CFG3	Configure to 0x00.
0x4D	1	ADC_CFG4	Configure to 0x03.

An interrupt will be generated after AD data conversion of each group of 4 channels. Relevant settings are as follows:

Interrupt Type	Program Entry Address	Trigger Flag	Interrupt Enable Control	Remark
AD interrupt	0x00AB	MUX_SEL1.7	IEN2.5	After interrupt service, software is required to clear the corresponding interrupt trigger flag. Check whether ADC_SET.6 (corresponding to AD_CH0-3) or ADC_SET.5 (corresponding to AD_CH4-7) is set to determine which group of 4-channel data to read.

User software can poll ADC_SET.6 and ADC_SET.5 flags to check whether AD data has been updated and decide whether to read AD data, or read the data directly inside the AD interrupt service routine.

6.9 UART Communication Interface

The UART-related SFR control interfaces are shown in the table below.

SFR Name	Address	Description
MUX_SEL	0xC9	Bit =6: 1=UART pins are mapped to P0.4 and P0.5; 0=P0.4 and P0.5 function as general I/O ports, UART interface not routed out.
SCON0	0x98	UART control register, compatible with standard 8051, bit-addressable . Bit7=SM0, Bit6=SM1, Bit5=SM2 (multiprocessor communication bit), Bit4=REN0, Bit3=TB80, Bit2=RB80, Bit1=TI0, Bit0=RI0.
SBUF0	0x99	UART data register for transmit and receive.
ADCON	0xD8	Baud rate generator selection. 0x00=Timer T1 (standard 8051 mode); 0x80 =use SREL0H:L.
PCON	0x87	Bit7=SMOD, baud rate doubler. 0=no doubling; 1=baud rate doubled.
SREL0H	0xBA	When ADCON=0x80, SREL0H:L configures baud rate without occupying Timer T1. SMOD=0: SREL0H:L=1024-CPU_Freq/(64 × Baudrate)SMOD=1:
SREL0L	0xAA	SREL0H:L=1024- CPU_Freq/(32 × Baudrate) CPU main frequency=236 MHz.

UART interrupt related settings are listed below.

Interrupt Type	Program Entry Address	Trigger Flag	Interrupt Enable Control	Remark
UART interrupt	0x0023	RIO (SCON0.0) T10 (SCON0.1)	IEN0.4	Software must clear the corresponding interrupt trigger flag after interrupt service routine.

6.10 Interrupt System

6.10.1 Interrupt Control SFR

The T5S0 OS CPU supports a total of 11 interrupts. The list of related control SFRs is shown below:

SFR Name	Address	Description
IEN0	0xA8	Interrupt enable controller 0, bit-addressable . Bit7 EA: Global interrupt enable bit. 0=All interrupts disabled; 1=Interrupts are enabled or disabled by their respective local enable bits. Bit6: Must write 0. Bit5 ET2: T2 timer interrupt enable bit. Bit4 ES0: UART interrupt enable bit. Bit3 ET1: T1 timer interrupt enable bit. Bit2 EX1: External interrupt 1 (Pin P1.7) enable bit. Bit1 ET0: T0 timer interrupt enable bit.

		Bit0 EX0: External interrupt 0 (Pin P1.6) enable bit.
IEN1	0xB8	Interrupt enable controller 1. Must be written as 0x00.
IEN2	0x9A	Interrupt enable controller 2. Bit7~Bit6: Must write 0. Bit5 EADC: ADC end-of-conversion interrupt enable bit. Bit4 EPWM3: PWM3 interrupt enable bit. Bit3 EPWM2: PWM2 interrupt enable bit. Bit2 EPWM1: PWM1 interrupt enable bit. Bit1 EPWM0: PWM0 interrupt enable bit. Bit0: Must write 0.
IEN3	0xD1	Interrupt enable controller 3. Must be written as 0x00.
IP0	0xA9	Interrupt priority controller 0.
IP1	0xB9	Interrupt priority controller 1.

6.10.2 Interrupt Priority Rules of T5S0 OS CPU

The interrupt priority of T5S0 OS CPU is handled in accordance with the following rules:

1. The 11 interrupts are divided into 6 groups, with each group containing 1-2 interrupts. The priority inside each group is fixed. For instance, within the same group, External Interrupt 1 has higher priority than PWM1 Interrupt, as shown in the table below.

Group	Corresponding IP0 Bit	Corresponding IP1 Bit	Corresponding Interrupt		
			High Priority	Medium Priority	Low Priority
G0	.0	.0	External Interrupt 0		
G1	.1	.1	T0 Timer Interrupt	PWM0 Interrupt	
G2	.2	.2	External Interrupt 1	PWM1 Interrupt	
G3	.3	.3	T1 Timer Interrupt	PWM2 Interrupt	
G4	.4	.4	UART Interrupt	PWM3 Interrupt	
G5	.5	.5	Timer Interrupt	ADC End-of-Conversion Interrupt	

2. There are 4 priority levels among the 6 groups, configurable via corresponding bits of IP0 and IP1 as shown below.

Inter-Group Priority	Corresponding IP0 Bit	Corresponding IP1 Bit
3 (Highest)	1	1
2	1	0
1	0	1
0 (Lowest)	0	0

Example: To set the T2 Timer Interrupt and ADC End-of-Conversion Interrupt in Group G5 to the highest priority, configure IP1=0x20 (IP1.5=1), IP0=0x20 (IP0.5=1).

3. When all configured priority levels are identical (IP1=0x00, IP0=0x00), interrupts are processed with group G0 having the highest priority and group G5 the lowest. The interrupt priority weight table for uniform configuration is as follows:

Weight Value	10	9	8	7	6	5	4	3	2	1	0
Priority	Highest										Lowest
Interrupt	EX0	T0	PWM0	EX1	PWM1	T1	PWM2	UART	PWM3	T2	ADC

4. High-priority interrupts can preempt low-priority interrupts. In other words, an interrupt with a smaller weight value can be interrupted by one with a larger weight value. A maximum of four nesting levels is supported.

Note: The T5S0 OS CPU delivers high processing speed, executing an average of 160 to 200 instructions per microsecond. Interrupt service routines have short execution time and already provide very high real-time performance. Interrupt nesting is not recommended for users, as it complicates the program architecture. It is advised to disable global interrupts (EA=0) at the start of each interrupt service routine and re-enable them (EA=1) upon exit.

Revision Record

Version	Date	Description	Editor
V1.1	2026-09-23	First Release	Chen Xian

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