LI12720T050TA3098

5.0 inch, 720*1280 pixels resolution, MIPI interface, IPS-TFT-LCD

Disclaimer：The product design is subject to alternation and improvement without prior notice.

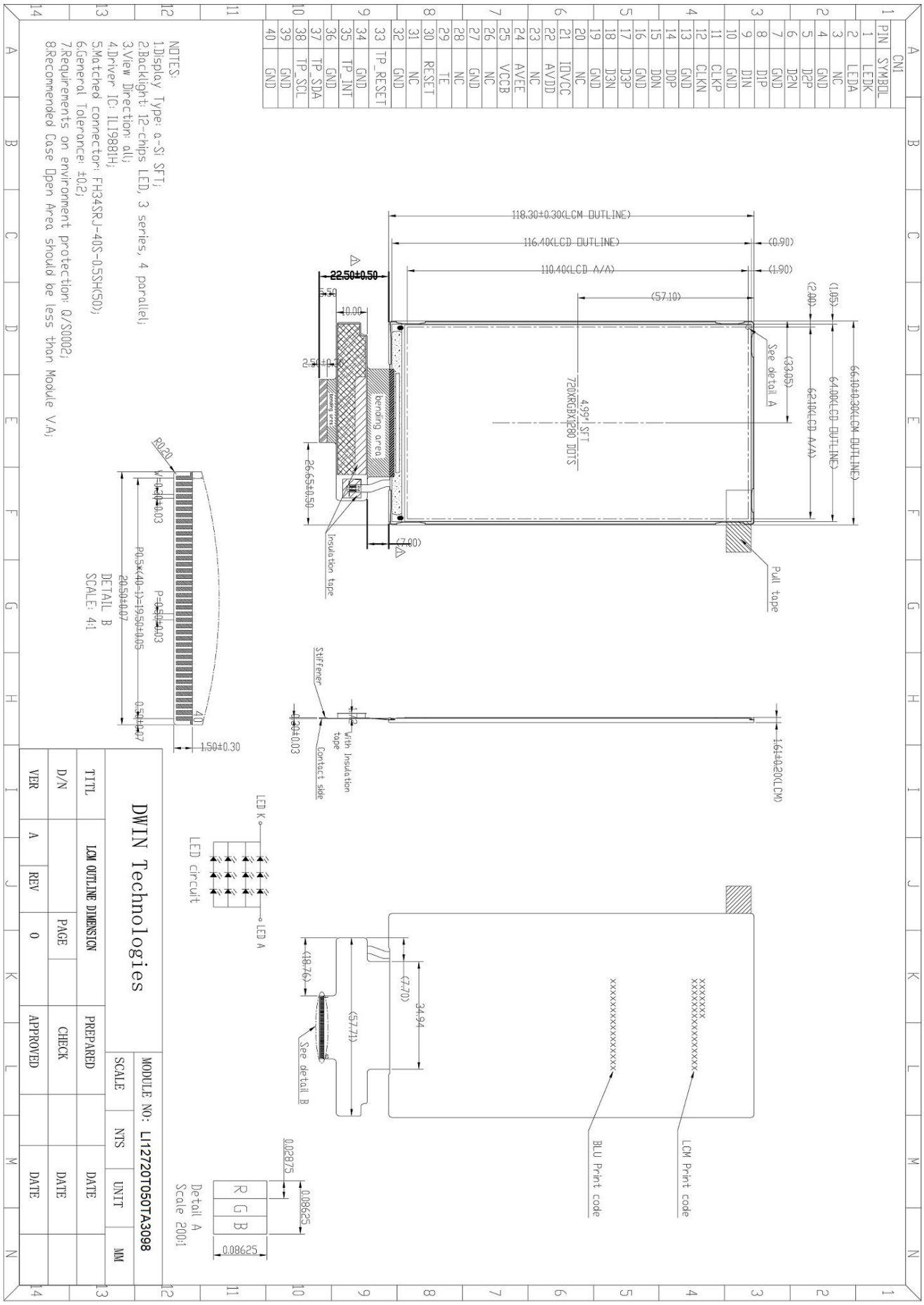
Table of Contents

1 General Feature

Feature		Description	Unit
Display Spec.	Size	5.0	inch
	Resolution	720(H)*1280(V)	pixels
	Pixel Configuration	RGB stripe	-
	Pixel Pitch	0.08625(W)*0.08625(H)	mm
	Viewing Direction	ALL	-
Mechanical Characteristics	Outside Dimension	66.10(W)*118.30(H)*1.61(D)	mm
	Active Area	62.10(W)*110.40(H)	mm
	Luminance	300	cd/m²
	CTP Touch Method	Finger	-
	Number of Simultaneous Touches	2	-
	Minimum Touch Area	Φ7	
	CTP Structure	Incell(Without Cover Lens)	-
	LED Numbers	12 LEDS	-
	Pin Order	From left to right 40PIN_0.5mm	-
Electrical Characteristics	Interface	MIPI	-
	CTP Interface	IIC	-
	Color Depth	16.7M	colors
	Driver Condition	-	V
	Driver IC	ILI9881H	-
Temperature Range	Operating Temp.	-20~70	℃
	Storage Temp.	-30~80	℃

Note: Requirements on Environmental Protection: RoHS.
You can use dynamic screen saver wallpapers to avoid afterimages caused by fixed paper display for a long time.

2 Mechanical Drawing



3 Input/Output Terminals

Pin NO.	Symbol	I/O	Function	Remark
1	LEDK	P	LED cathode pin	
2	LEDA	P	LED anode pin	
3	NC	--	Not connect	
4	GND	P	Power Ground	
5	D2P	I	MIPI DSI DATA2 Positive	
6	D2N	I	MIPI DSI DATA2 Negative	
7	GND	P	Power Ground	
8	D1P	I	MIPI DSI DATA1 Positive	
9	D1N	I	MIPI DSI DATA1 Negative	
10	GND	P	Power Ground	
11	CLKP	I	MIPI DSI CLOCK Positive	
12	CLKN	I	MIPI DSI CLOCK Negative	
13	GND	P	Power Ground	
14	D0P	I	MIPI DSI DATA0 Positive	
15	D0N	I	MIPI DSI DATA0 Negative	
16	GND	P	Power Ground	
17	D3P	I	MIPI DSI DATA3 Positive	
18	D3N	I	MIPI DSI DATA3 Negative	
19	GND	P	Power Ground	
20	NC	--	Not connect	
21	IOVCC	P	Power supply to interface pins(1.8V)	
22	AVDD	P	Positive input analog power for driver IC use(6.0V)	
23	NC	--	Not connect	
24	AVEE	P	Negative input analog power for driver IC use(-6.0V)	
25	VCCB	P	Power supply to level shift IC(3.3V). If not used, please let it open	
26	NC	--	Not connect	
27	GND	P	Power Ground	
28	NC	--	Not connect	
29	TE	O	Tearing effect output signal. If not used, please let this pin open.	
30	RESET	I	LCM Reset pin, the LCD driver is initialized when RESET active low	
31	NC	--	Not connect	
32	GND	P	Power Ground	
33	TP_RESET	I	Reset pin, the TP is initialized when RESET active low	
34	GND	P	Power Ground	
35	TP_INT	O	Communication interrupt	
36	GND	P	Power Ground	
37	TP_SDA	I/O	I2C data	
38	TP_SCL	I	I2C clock	
39	GND	P	Power Ground	
40	GND	P	Power Ground	

4 Electrical Characteristics

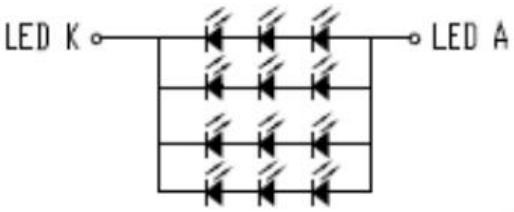
4.1 Driving TFT LCD Panel

Item	Symbol	Min	Typ.	Max.	Unit	Remark
Logic Operating Voltage	IOVCC	1.7	1.8	1.9	V	
Operating Voltage	AVDD	5.9	6.0	6.1	V	
	AVEE	-6.1	-6.0	-5.9	V	
	VCCB	3.2	3.3	3.4	V	
Input Signal Voltage Low Level	V_{IL}	0	-	0.3* IOVCC	V	
Input Signal Voltage High Level	V_{IH}	0.7* IOVCC	-	IOVCC	V	
Output Signal Voltage Low Level	V_{OL}	0	-	0.2* IOVCC	V	
Output Signal Voltage High Level	V_{OH}	0.8* IOVCC	-	IOVCC	V	

4.2 LED Backlight Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Voltage for LED Backlight	VL	8.4	9.6	10.8	V	
Current for LED Backlight	IL	-	80	100	mA	
Backlight Power Consumption	W_{BL}	-	768	1080	mW	3 series, 4 parallel
Luminance(with LCD)	Lv	-	300	-	cd/m²	If=80mA
LED Life-Time	Hr	10000	20000	-	hrs	

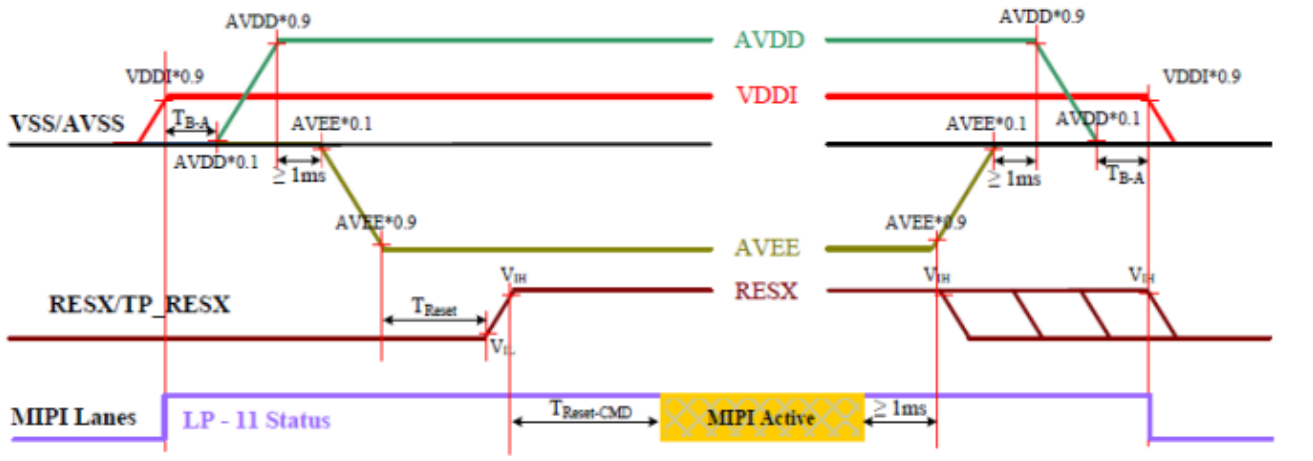
Note: 12 LEDs (3 LEDs Serial,4 ways Parallel)



LED circuit

5 Timing Characteristics

5.1 Power on/off Sequence



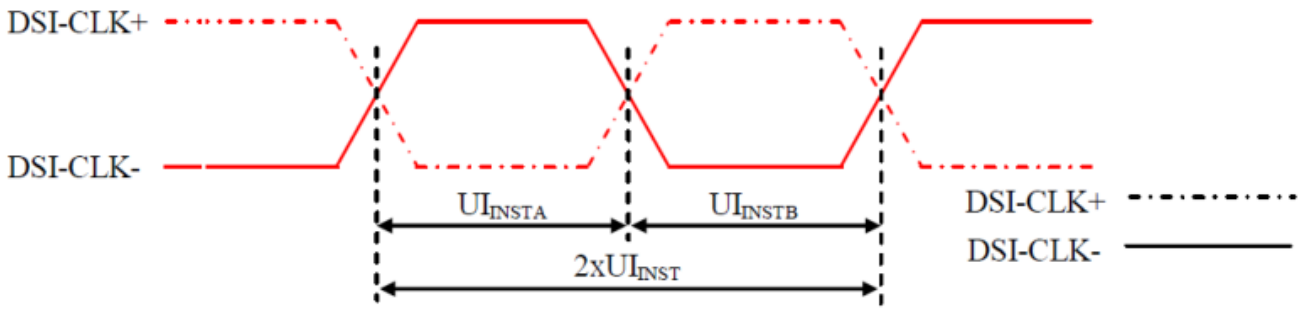
Power on/off Sequence

Symbol	Characteristics	Min.	Typ.	Max.	Units
TRise	External Power Rise Time	0.2	-	20	ms
TFall	External Power Fall Time	0.2	-	20	ms
TB-A	Delay Time between Two External Power	2	5	-	ms
TReset	Delay Time between External Power and Reset	4	10	-	ms
TReset-CMD	Reset to First Command in Display Sleep in Mode	10	-	-	ms

Timing Relation of Power on/off Sequence

5.2 DSI Timing Characteristics

5.2.1 High Speed Mode-Clock Channel Timing



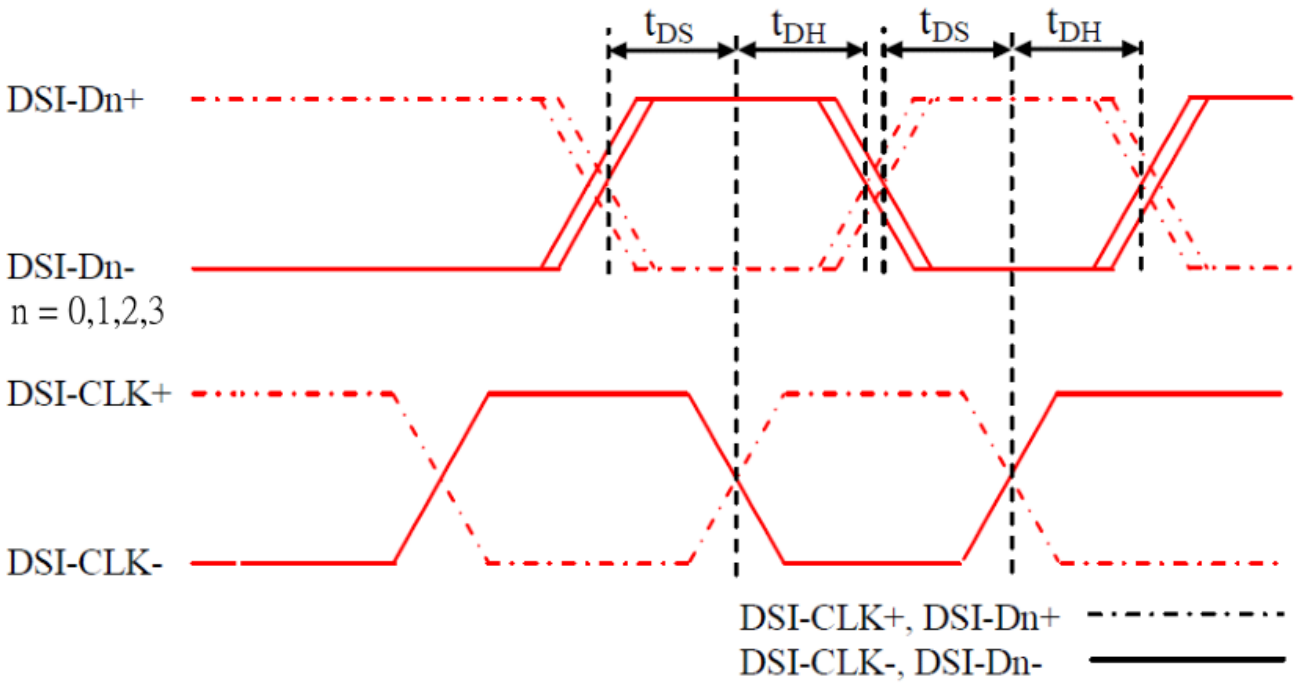
DSI Clock Channel Timing

Signal	Symbol	Parameter	Min.	Max.	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	2	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	1	12.5	ns

Note: $UI_{INST} = UI_{INSTA} = UI_{INSTB}$

DSI Clock Channel Timing

5.2.2 High Speed Mode-Data Clock Channel Timing

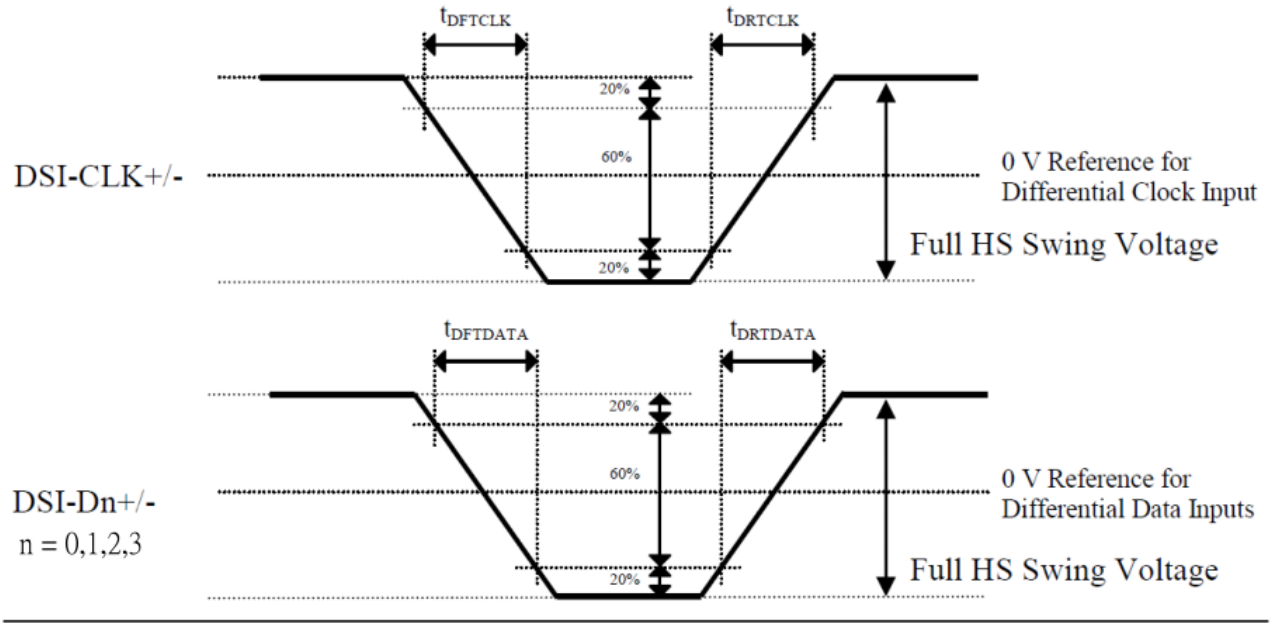


DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min.	Max.
DSI-Dn+/- (n=0,1,2,3)	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

DSI Data to Clock Channel Timings

5.2.3 High Speed Mode-Rise and Fall Timings



Rise and Fall Timings on Clock and Data Channels

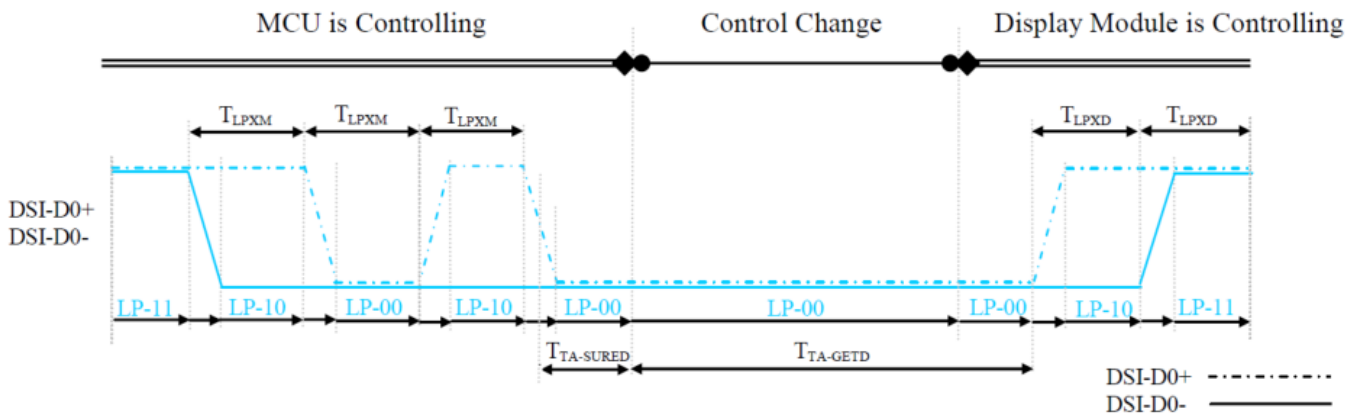
Parameter	Symbol	Condition	Specification		
			Min.	Typ.	Max.
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI

Rise and Fall Timings on Clock and Data Channels

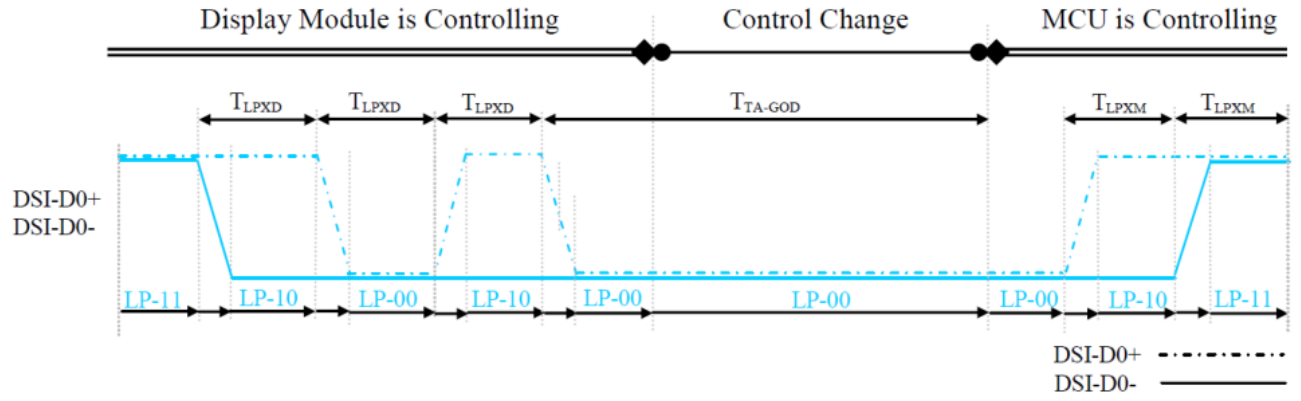
Note:

The display module has to meet timing requirements, what are defined for the transmitter(MCU)on MIPI D-Phy Standard.

5.2.4 Low Speed Mode-Bus Turn Around



BTA from the MCU to the Display Module



BTA from the Display Module to MCU

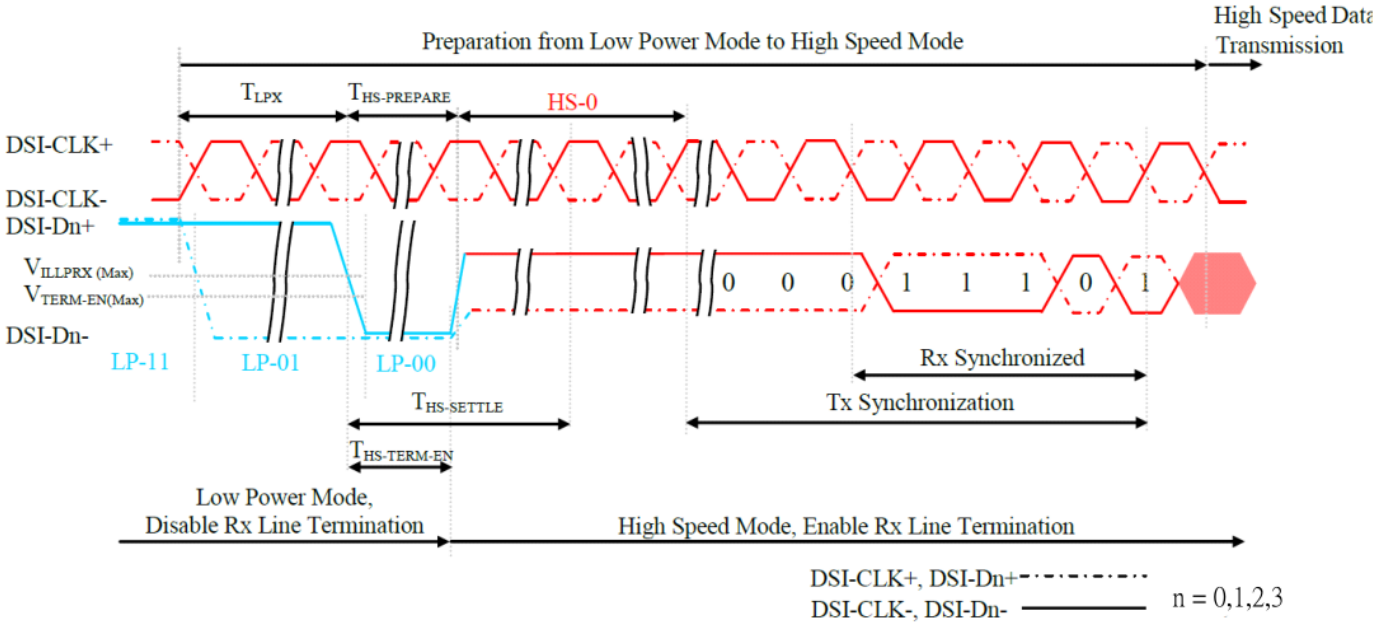
Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI2882N)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI2882N) ➔ MCU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (ILI2882N) starts driving	T_{LPXD}	$2*T_{LPXD}$	ns

Low Power State Period Timings-A

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI2882N)	$5*T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MCU	$4*T_{LPXD}$	ns

Low Power State Period Timings-B

5.2.5 Data Lanes from Low Power Mode to High Speed Mode

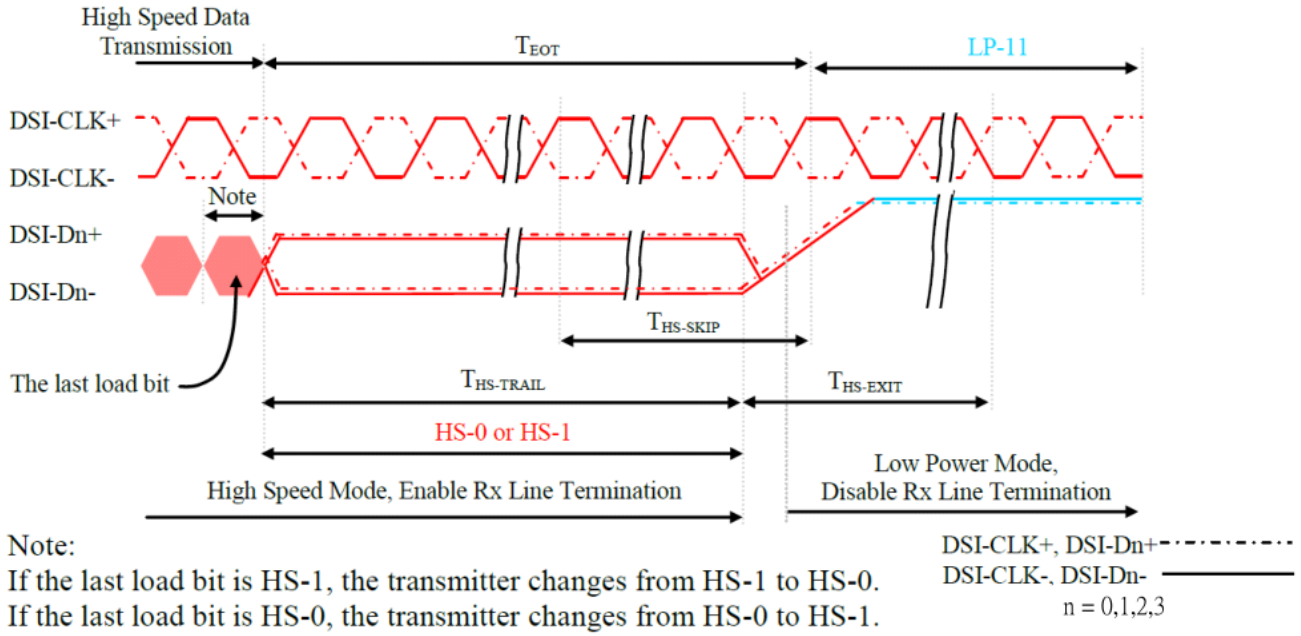


Data Lanes-Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- (n=0,1,2,3)	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Data Lanes-Low Power Mode to High Speed Mode Timings

5.2.6 Data Lanes from High Speed Mode to Low Power Mode



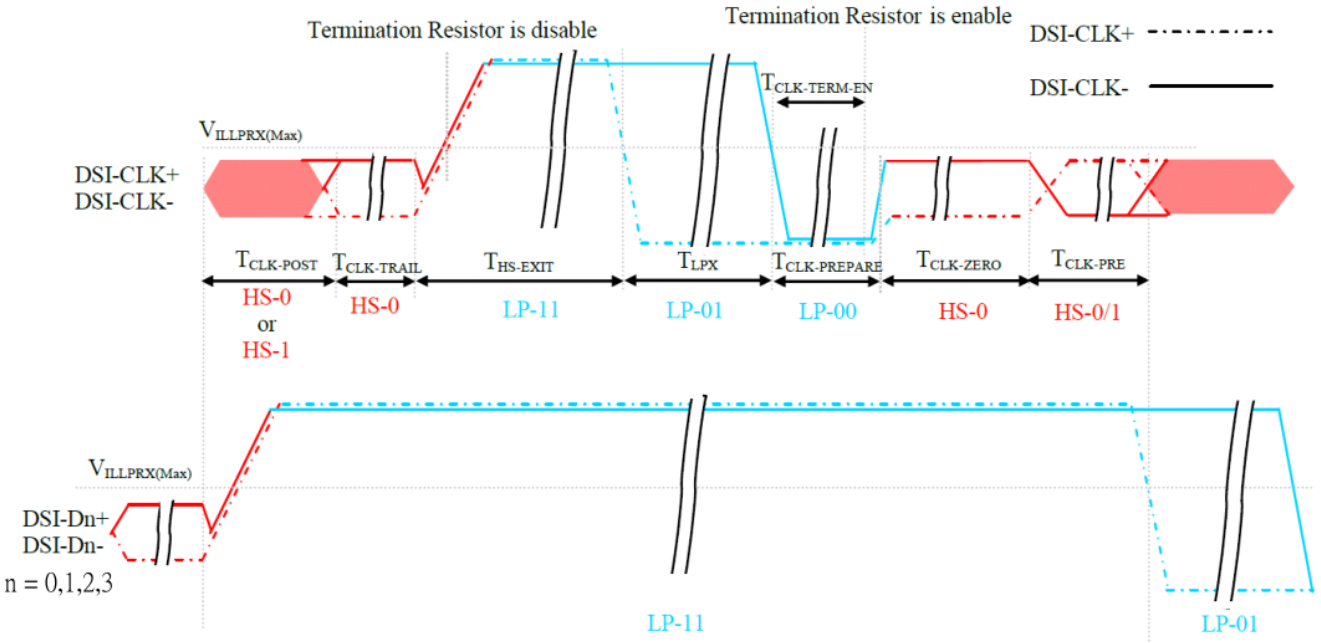
Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Data Lanes-High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-SKIP}$	Time-Out at Display Module (ILI2882N) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(8*UI, 60ns+ 4*UI)	-	ns

Data Lanes-High Speed Mode to Low Power Mode Timings

5.2.7 DSI Clock Burst-High Speed Mode to/from Low Power Mode

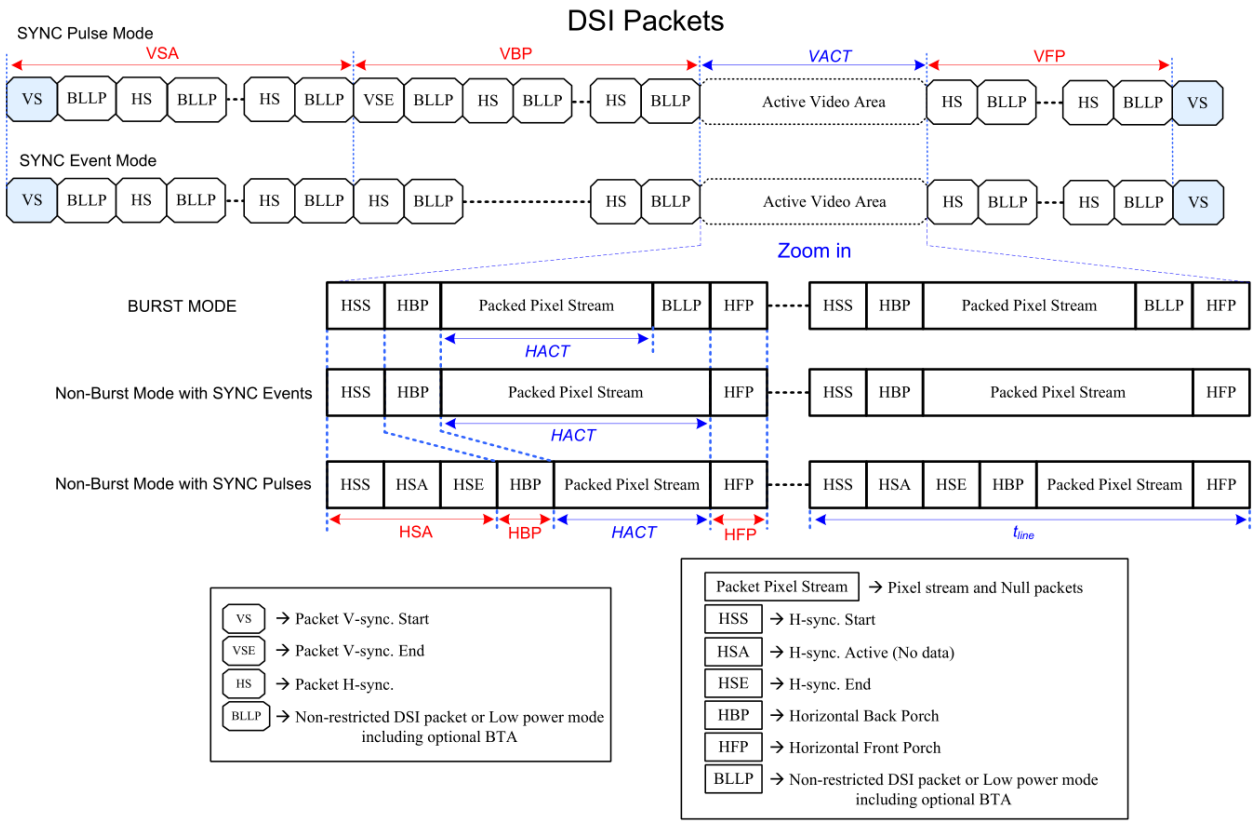


Clock Lanes-High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Clock Lanes-High Speed Mode to/from Low Power Mode Timings

5.2.8 Timing for DSI Video Mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA Note 6, 7	2	-	-	Line
Vertical Back Porch	VBP Note 6, 7	16	-	-	Line
Vertical Front Porch	VFP Note 6, 7	20	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch	HSA + HBP+ HFP	0.5	-		us
Active pixels per line	HACT	-	720	-	Pixel
Bit Rate	BRbps	-	-	Note 5	Mbps/lane

1 UI = 1/Bit rate

HAS(pixel) = (tHSA*lane number) / (UI* pixel format)

HBP(pixel) = (tHBP*lane number) / (UI* pixel format)

HFP(pixel) = (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 880Mbps/lane, 1UI=1.13ns, Frame rate=60.2Hz, VACT=1280, VSA=4, VBP=4, VFP=4, HACT=720, HSA=20, HBP=70, HFP=90, $Lane_{num}$=4(lane), Pixel Format=24(bit).

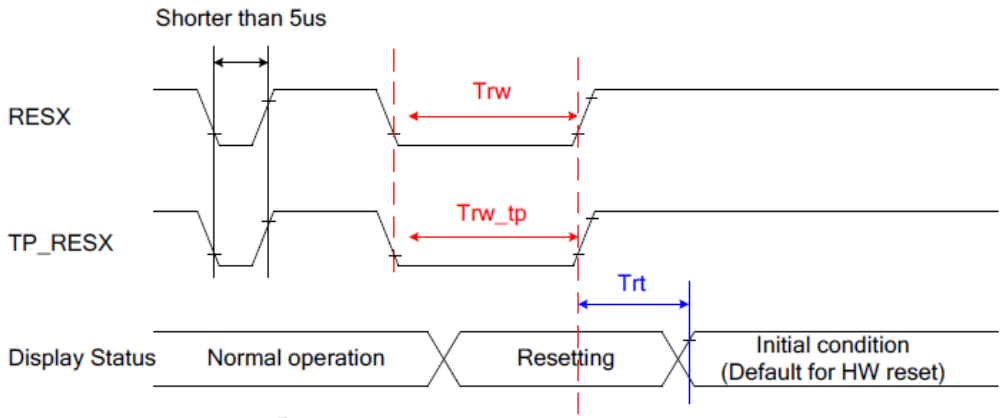
Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to "4.3 DSI System Interface".
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting is 60 Hz.
5. Please reference to the following table.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP.
7. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	666 Mbps	532 Mbps	466 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	666 Mbps	532 Mbps	466 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	1000 Mbps	800 Mbps	700 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	1000 Mbps	800 Mbps	700 Mbps

Limited Clock Channel Speed

5.2.9 Reset Timings



Signal	Symbol	Parameter	Min	Max	Unit
RESX	Trw	Reset pulse duration	10	-	us
	Trt	Reset cancel	35 (Note 1,5)	-	ms
			150 (Note 1,6,7)	-	ms
TP_RESX	Trw_tp	Reset pulse duration	1	-	us

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM to registers. This loading is done every time when there is H/W reset cancel time (Trt) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the following table.

RESX	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and return to default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown in following figure.

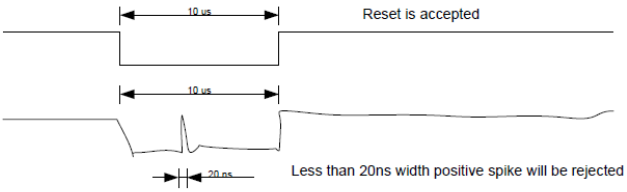


Figure 98. Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending other commands. Also Sleep Out command (11h) cannot be sent for 120msec.

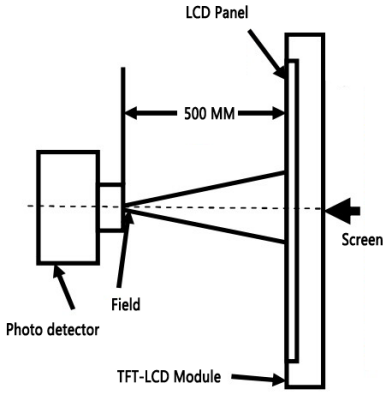
6 Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle	Top	CR≧10	70	85	-	Deg.	Note 2,3
	Bottom		70	85	-		
	Left		70	85	-		
	Right		70	85	-		
Contrast Ratio	CR		700	900	-		Note 3
Color Chromaticity (CIE1931)	Wx	θ=0°	0.253	0.283	0.313		Note 1,5
	Wy		0.272	0.302	0.332		
	Rx		0.598	0.628	0.658		
	Ry		0.303	0.333	0.363		
	Gx		0.285	0.315	0.345		
	Gy		0.579	0.609	0.639		
	Bx		0.111	0.141	0.171		
	By		0.022	0.052	0.082		
Uniformity	U		70	80	-	%	
Color Gamut	NTSC		65	70	-	%	
Response Time	T_{ON}	25℃	-	30	40	ms	
	T_{OFF}						

Test conditions:
IF= 80mA, and the ambient temperature is 25℃.

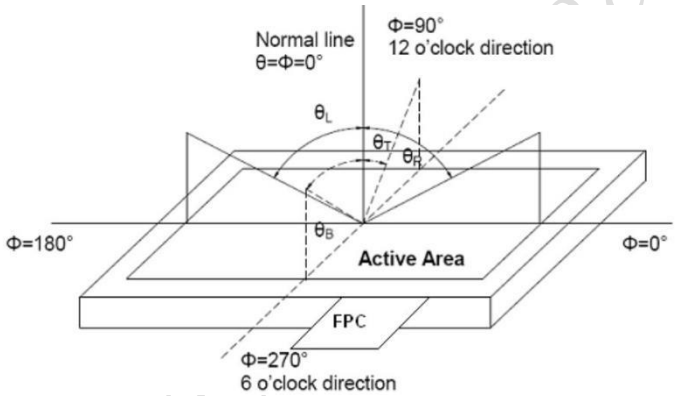
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of LCD.



Note 2: Definition of viewing angle range and measurement system.

The viewing angle is measured at the center point of the LCD by BM-7A.

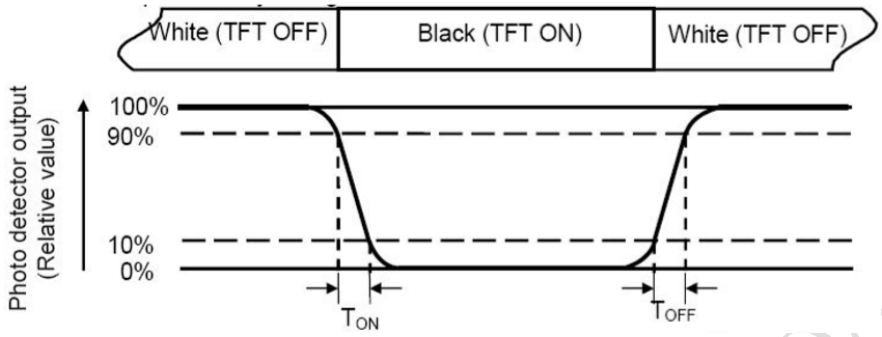


Note 3: Definition of color temperature.

When the radiation of the light source is exactly the same in the visible region and the absolute blackbody, the temperature of the blackbody is called the color temperature of the light source. Color temperature is an index to measure the degree of light source color (cold color, warm color). Warm color < 3300K, intermediate color 3300 ~ 5000K, cold color > 5000K.

Note 4: Definition of response time.

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Time ON (TON) is the time between photo detector output intensity changed from 90% to 10%. And time off (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931).

Color coordinates measured at center point of LCD.

Note 6: Definition of luminance.

Measure the luminance of white state at center point.

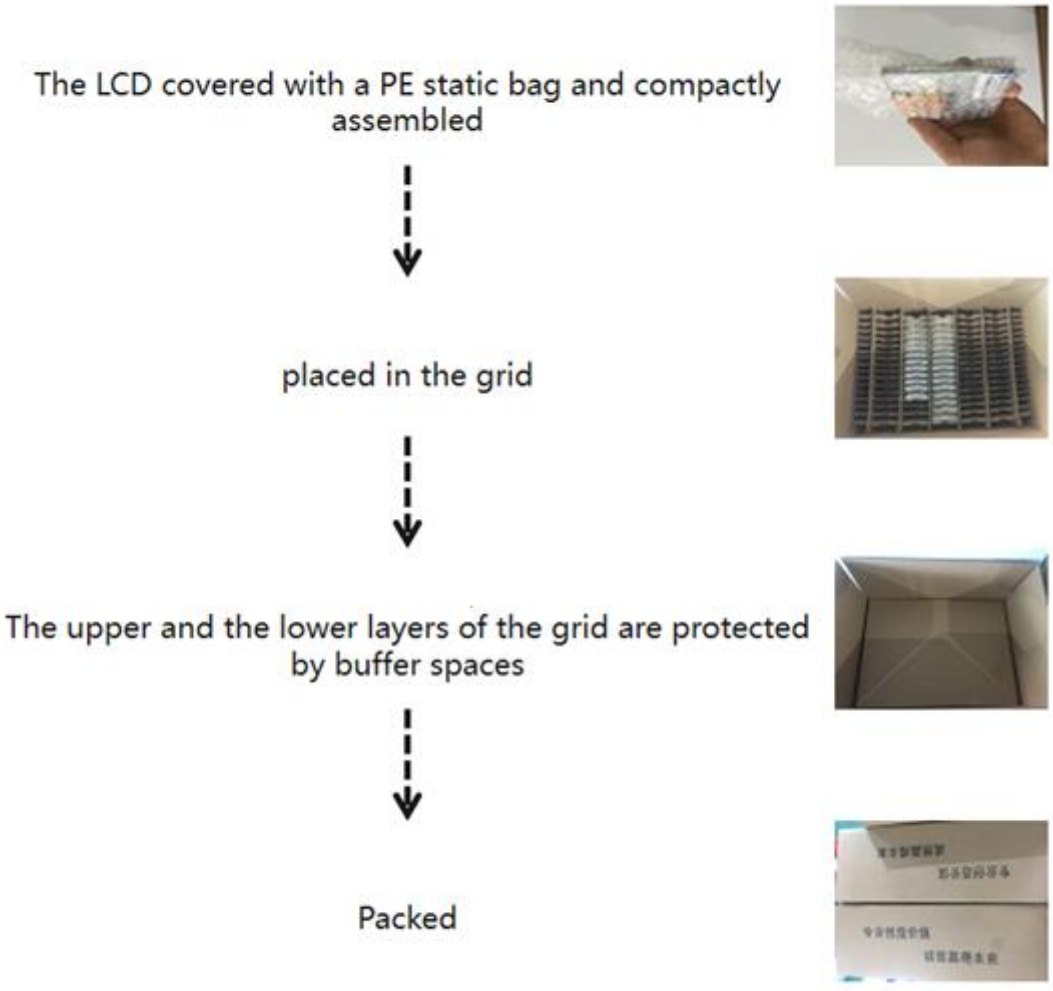
7 Environmental Reliability Test

NO	Test Item	Condition	Remarks
1	High Temperature Operation	Ta=+70℃,96hours	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	Ta=-20℃,96hours	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta=+80℃,96hours	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	Ta=-30℃,96hours	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity	Ta=+60℃,90% RH max,96hours	IEC60068-2-78 :2001 GB/T2423.3-2006
6	Thermal Shock (non-operation)	-20℃ 30 min~+70℃ 30 min, 5min 100 Cycles	Start with cold temperature, End with high temperature, IEC60068-2-14:1984, GB 2423.22-2002
7	ESD(non-operation)	C=150pF, R=330Ω,5point/panel Air: ±8kv,5times; Contact: ±4kv5times; （Environment:15℃~35℃,30%~60%, 86Kpa~106Kpa）	IEC61000-4-2:2001 GB/T 17626.2-2006
8	Vibration Test	Frequency range:10~55Hz， Stroke:1.5mm, Sweep:10Hz~55Hz~10Hz，2h for x,y,z（total 6h）	IEC60068-2-6:1982 GB/T 2423.10-1995
9	Mechanical Shock (Non OP)	Half Sine Wave 60G ,6ms,±X,±Y,±Z 3times for each direction	IEC60068-2-27:1987 GB/T 2423.5-1995
10	Package Drop Test	Height: 60 cm,1 corner, 3edges, 6 surfaces	IEC60068-2-32:1990 GB/T 2423.8-1995

8 Packing Capacity & Dimension

Dimension			
Dimension(mm)	66.10(W)*118.30(H)*1.61(D)		
Net Weight	-		
Packing Capacity			
Size	**LCD Size and Resolution**	**Layer**	**Quantity(Pcs)**
220mm(L)x160mm(W)x47mm(H)	5.0 inch 720*1280	1	1
450mm(L)x350mm(W)x300mm(H)	5.0 inch 720*1280	2	120

Packing instruction：
The LCD is placed in the grid, covered with a PE static bag and compactly assembled, the upper and the lower layers of the grid are protected by buffer spaces.



9 Appearance Inspection

9.1 General rules for inspection

9.1.1 Anti-static wearables (anti-static wristbands, gloves) must be worn during the inspection.

9.1.2 Do not use bare hands to touch the position of the device, golden fingers, and the surface of the screen to prevent the sweat from human hands from causing oxidation and affecting the appearance.

9.1.3 It is forbidden to stack products out of specification and handle them with care to avoid damage to components.

9.1.4 The repaired products need to be inspected to prevent rosin and tin slag from exceeding the specifications.

9.1.5 When technical documents and process documents have specific requirements for products, the technical documents and process documents shall be the main requirements.

9.2 Inspection conditions

9.2.1 The conditions of display function check

Angle: ±5°;

Inspection method: visual inspection. The inspection object is 30-40cm away from the light source, and the eye is 30-40cm away from the inspection object;

Illumination: 300-500Lux;

Inspection time: 5-10S.

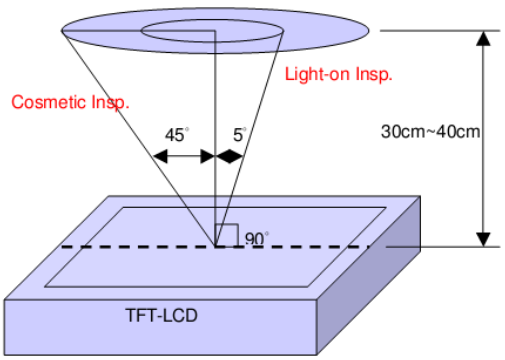
9.2.2 Visual inspection conditions

Angle: ±45°;

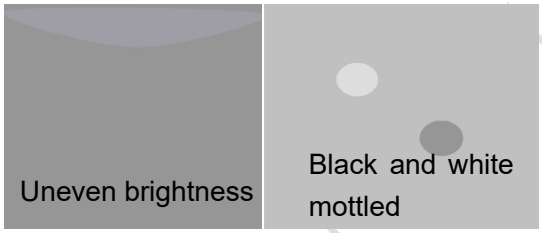
Inspection method: visual inspection. The inspection object is 30-40cm away from the light source, and the eye is 30-40cm away from the inspection object;

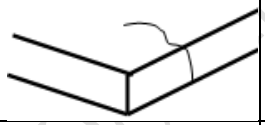
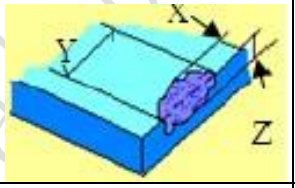
Illumination: 800-1500Lux;

Inspection time: 5-10S.



9.3 Inspection standards

Type	Test Items	Judgement Standard	Defect Category
Display state	Dead pixels	No dead pixels	
	mura	From different angles, the brightness is required to be uniform. Under the 64-level grayscale or pure black interface, there should be no uneven display brightness within the viewing angle range of 45° through 6% ND FILTER. Y series (TV film) LCD screen does not have specific requirements, and the picture inspection does not affect the display as qualified.  Uneven brightness　Black and white mottled	Slight defect
	Light leakage	Under the 64-level grayscale or pure black interface, there should be no obvious light leakage within the viewing angle range of 45° by visual inspection or through 6% ND FILTER. Y series (TV LCD screen) series can be without obvious visual defects.	Slight defect
	Linear foreign bodies	1. W≤0.05, L≤2mm, negligible; 2. 0.05mm＜W≤0.1mm, L≤2mm, N≤3; 3. W＞0.1mm, L＞2mm, not allowed.	Slight defect
Screen surface	Within the effective area	Spotted: 1. D≤0.2mm and it is not a piece, it is not counted; 2. 0.2mm＜D≤0.5mm, N≤3; 3. D>0.5mm, L>0.5mm, W>0.5mm are not allowed; (The spotted foreign objects shall not exceed the point-line gauge D=0.5, and the black dot coverage shall be checked, and the spotted foreign objects shall be judged within the range of D=0.5)	Slight defect

	Foreign objects Scratch Air bubbles	Linear: 1. W≤0.05, L≤2mm, ignored; 2. 0.05＜W≤0.1mm, L≤2mm, N≤3; 3. W>0.1mm, L>2mm, not allowed.	
	Outside the effective area Foreign objects Scratches Air bubbles	。 Foreign objects are not checked, and bubbles are not allowed to D>1mm; Non-inductive scratches of no more than 0.1×8mm are allowed.	Slight defect
	Crack	Not allowed. 	Slight defect
	Notch	1. Does not affect the appearance from the front; 2. Does not affect the relevant alignment; 3. X≤1mm, Y≤1mm, N≤2. 	Slight defect
	Glass side Foreign objects Dirty	。 1. The foreign body on the side is not controlled; 2. The paint pen marks on the side are not controlled; 3. Side oily note printing is not allowed.	Slight defect
FPC	Cracks Goldfinger crease	Not allowed.	Heavy deficit
	Crease	Slight creases are not controlled; The crease is whitish and has lines, which is not allowed.	Heavy deficit
	Top wound, stab wound	No damage to the line, D≤0.2mm; Damage to the line is not allowed.	Heavy deficit
	Scratch	Slight scratches on the surface are not controlled; Damage to the line is not allowed.	Heavy deficit
	Goldfinger scratch	W≤0.05mm, no control; W＞0.05mm, not allowed; Test probe tip marks are not controlled.	Heavy deficit
	Component	Under-soldering, over-soldering and false soldering are not allowed.	Heavy deficit

10 Precautions for Use of LCD Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, Can only use LCD dedicated cleaner, the following organic solvent can not be used:

- Isopropyl alcohol
- Ethyl alcohol
- Ketone
- Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an

10.1.9 optimum work environment.

10.1.9.1 Be sure to ground the body when handling the LCD Modules.

10.1.9.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.9.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.9.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:
Temperature: 0℃ ~ 40℃ Relatively humidity: ≤80%.

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

10.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

11 LCD Introduction

11.1 Process capacity

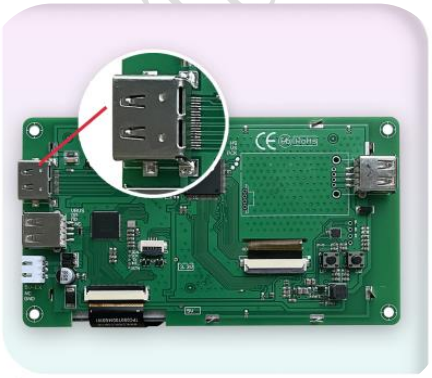
DWIN adopts original class A glass and the entire production is in the park from cleaning, cutting, bonding, and laminating of large glass to backlight assembly, quality inspection, and aging.

There are 12,000 square meters of clean workshop, with a monthly production capacity of about 2.5 million pieces.

11.2 ODM service

Based on LCD products of 1.5~21.5 inches, DWIN provides the following customization services.

1、LCD HDMI interface customization.



HDMI interface

2、Special screen customization such as high brightness, ultra-wide temperature and strong electromagnetic protection.

High luminance
(up to 1200nit)

Ultra-wide temperature
(-40~85℃)

Strong electromagnetic protection

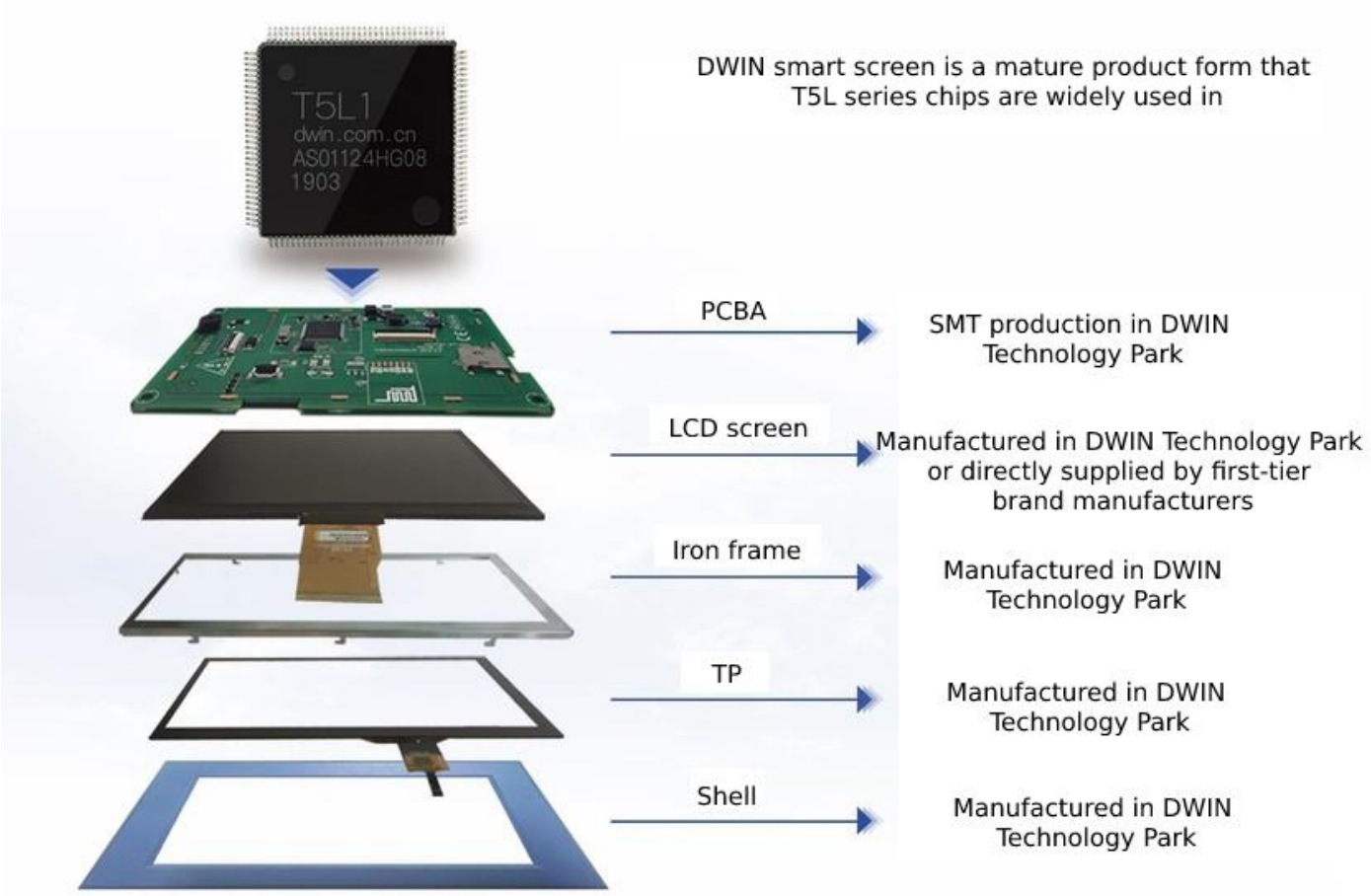
3、Lamination customization service of LCD + TP.

LCM+RTP

LCM+CTP

4、Customization service of DWIN self-developed T5L ASIC+ LCD + TP.

5、Smart screen finished product customization.



Please contact our sales staff for other customization needs.

Record of Revision

Rev	Date	Description	Editor
00	2021-09-02	First Release	Ouyang Kaixing
01	2023-01-29	Full English Version	Chen Xian
02	2023-02-06	Add Product Picture	Chen Xian
03	2023-02-22	Update Packing Capacity	Chen Xian

Please contact us if you have any questions about the use of this document or our products, or if you would like to know the latest information about our products:

Customer service tel: +86 400 018 9008

Customer service email: dwinhmi@dwin.com.cn

DWIN developer forum: https://forums.dwin-global.com/index.php/forums/

Thank you all for continuous support of DWIN, and your approval is the driving force of our progress!